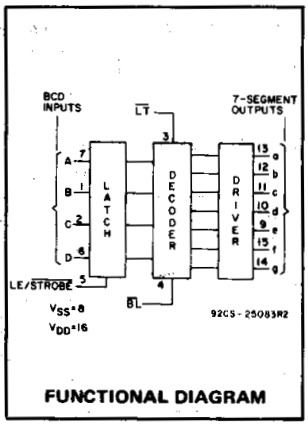
TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS072B – Revised July 2003

# CD4511B Types

## CMOS BCD-to-7-Segment Latch Decoder Drivers

High-Voltage Types (20-Volt Rating)

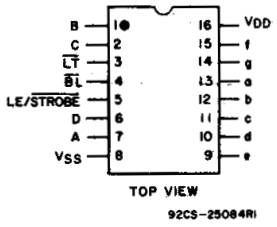

FUNCTIONAL DIAGRAM

■ CD4511B types are BCD-to-7-segment latch decoder drivers constructed with CMOS logic and n-p-n bipolar transistor output devices on a single monolithic structure. These devices combine the low quiescent power dissipation and high noise immunity features of RCA CMOS with n-p-n bipolar output transistors capable of sourcing up to 25 mA. This capability allows the CD4511B types to drive LED's and other displays directly.

Lamp Test ($\overline{LT}$), Blanking ($\overline{BL}$), and Latch Enable or Strobe inputs are provided to test the display, shut off or intensity-modulate it, and store or strobe a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplexing circuitry is used.

The CD4511B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

These devices are similar to the type MC14511.




CD4511B
TERMINAL ASSIGNMENT

*Features:*

- High-output-sourcing capability . . . . . up to 25 mA
- Input latches for BCD Code storage
- Lamp Test and Blanking capability
- 7-segment outputs blanked for BCD input codes > 1001
- 100% tested for quiescent current at 20 V
- Max. input current of 1 μA at 18 V, over full package-temperature range, 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings

*Applications:*

- Driving common-cathode LED displays
- Multiplexing with common-cathode LED displays
- Driving incandescent displays
- Driving low-voltage fluorescent displays

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
Voltages referenced to $V_{SS}$ Terminal) . . . . . -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55°C to +100°C . . . . . 500mW
For $T_A$ = +100°C to +125°C. . . . . Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100mW
OPERATING-TEMPERATURE RANGE ($T_A$) . . . . . -55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) . . . . . -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max . . . . . +265°C

**OPERATING CONDITIONS AT $T_A$ = 25°C Unless Otherwise Specified**

*For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges*

| Characteristic | $V_{DD}$ | Min. | Max. | Units |
|---|---|---|---|---|
| Supply-Voltage Range ($T_A$): (Full Package-Temperature Range) | – | 3 | 18 | V |
| Set-Up Time ($t_S$) | 5 | 150 | – | ns |
| | 10 | 70 | – | ns |
| | 15 | 40 | – | ns |
| Hold Time ($t_H$) | 5 | 0 | – | ns |
| | 10 | 0 | – | ns |
| | 15 | 0 | – | ns |
| Strobe Pulse Width ($t_W$) | 5 | 400 | – | ns |
| | 10 | 160 | – | ns |
| | 15 | 100 | – | ns |

3 COMMERCIAL CMOS HIGH VOLTAGE ICs

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | TEST CONDITIONS | | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $I_{OH}$ (mA) | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | −55 | −40 | +85 | +125 | +25 Min. | +25 Typ. | +25 Max. | |
| Quiescent Device Current: $I_{DD}$ Max. | – | – | – | 5 | 5 | 5 | 150 | 150 | – | 0.04 | 5 | μA |
| | – | – | – | 10 | 10 | 10 | 300 | 300 | – | 0.04 | 10 | |
| | – | – | – | 15 | 20 | 20 | 600 | 600 | – | 0.04 | 20 | |
| | – | – | – | 20 | 100 | 100 | 3000 | 3000 | – | 0.08 | 100 | |
| Output Voltage: Low-Level $V_{OL}$ Max. | – | – | 0,5 | 5 | 0.05 | | | | – | 0 | 0.05 | V |
| | – | – | 0,10 | 10 | 0.05 | | | | – | 0 | 0.05 | |
| | – | – | 0,15 | 15 | 0.05 | | | | – | 0 | 0.05 | |
| High-Level $V_{OH}$ Min. | – | – | 0,5 | 5 | 4 | 4 | 4.2 | 4.2 | 4.1 | 4.55 | – | V |
| | – | – | 0,10 | 10 | 9 | 9 | 9.2 | 9.2 | 9.1 | 9.55 | – | |
| | – | – | 0,15 | 15 | 14 | 14 | 14.2 | 14.2 | 14.1 | 14.55 | – | |
| Input Low Voltage, $V_{IL}$ Max. | – | 0.5,3.8 | | 5 | 1.5 | | | | – | – | 1.5 | V |
| | – | 1,8.8 | – | 10 | 3 | | | | – | – | 3 | |
| | – | 1.5,13.8 | | 15 | 4 | | | | – | – | 4 | |
| Input High Voltage, $V_{IH}$ Min. | – | 0.5,3.8 | | 5 | 3.5 | | | | 3.5 | – | – | V |
| | – | 1,8.8 | | 10 | 7 | | | | 7 | – | – | |
| | – | 1.5,13.8 | | 15 | 11 | | | | 11 | – | – | |
| Output Drive Voltage: High Level $V_{OH}$ Min. | 0 | | | 5 | 4.0 | 4.0 | 4.20 | 4.20 | 4.10 | 4.55 | – | V |
| | 5 | | | | | | – | – | – | 4.25 | – | |
| | 10 | | | | 3.80 | 3.80 | 3.90 | 3.90 | 3.90 | 4.10 | – | |
| | 15 | | | | | – | 3.50 | 3.50 | – | 3.95 | – | |
| | 20 | | | | 3.55 | 3.55 | 3.30 | – | 3.40 | 3.75 | – | |
| | 25 | | | | 3.40 | 3.40 | – | – | 3.10 | 3.55 | – | |
| | 0 | | | 10 | 9.0 | 9.0 | 9.20 | 9.20 | 9.10 | 9.55 | – | V |
| | 5 | | | | | – | – | – | – | 9.25 | – | |
| | 10 | – | – | | 8.85 | 8.85 | 9.00 | 9.00 | 9.00 | 9.15 | – | |
| | 15 | – | – | | – | – | – | – | – | 9.05 | – | |
| | 20 | – | – | | 8.70 | 8.70 | 8.40 | 8.40 | 8.60 | 8.90 | – | |
| | 25 | – | – | | 8.60 | 8.60 | – | – | 8.30 | 8.75 | – | |
| | 0 | – | – | 15 | 14.0 | 14.0 | 14.20 | 14.20 | 14.10 | 14.55 | – | V |
| | 5 | – | – | | – | – | – | – | – | 14.30 | – | |
| | 10 | – | – | | 13.90 | 13.90 | 14.0 | 14.0 | 14.0 | 14.20 | – | |
| | 15 | – | – | | – | – | – | – | – | 14.10 | – | |
| | 20 | – | – | | 13.75 | 13.75 | 13.50 | 13.50 | 13.70 | 13.95 | – | |
| | 25 | – | – | | 13.65 | 13.65 | – | – | 13.50 | 13.80 | – | |
| Output Low (Sink) Current, $I_{OL}$ Min. | – | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | – | mA |
| | – | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | – | |
| | – | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | – | |
| Input Current, $I_{IN}$ Max. | – | 0,18 | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | – | $±10^{-5}$ | ±0.1 | μA |

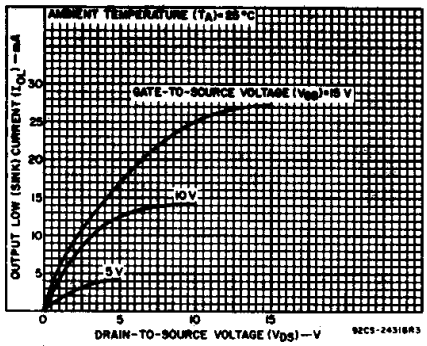



*Fig. 1 – Typical output low (sink) current characteristics.*

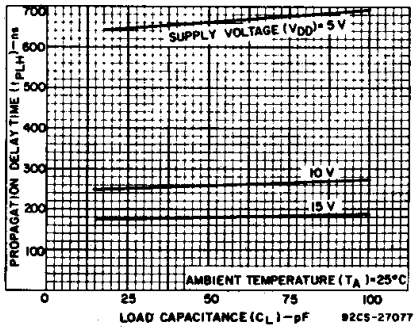



*Fig. 2 – Typical data-to-output, low-to-high-level propagation delay time as a function of load capacitance.*

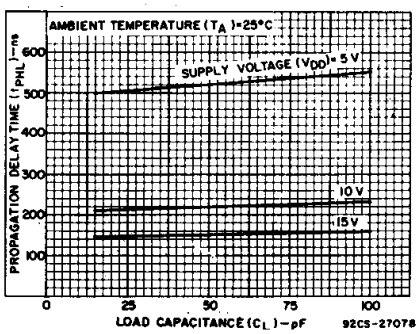



*Fig. 3 – Typical data-to-output, high-to-low-level propagation delay time as a function of load capacitance.*

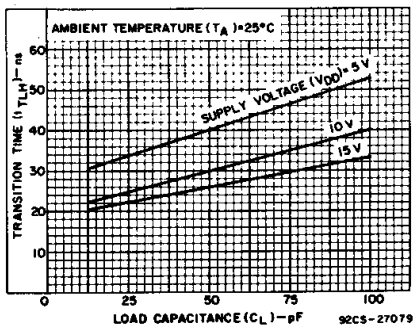



*Fig. 4 – Typical low-to-high-level transition time as a function of load capacitance.*

**DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A$ = 25°C, Input $t_r$, $t_f$ = 20 ns, $C_L$ = 50 pF, $R_L$ = 200 kΩ**

| CHARACTERISTIC | Test Conditions | LIMITS All Packages | | | UNITS |
|---|---|---|---|---|---|
| | $V_{DD}$ Volts | Min. | Typ. | Max. | |
| Propagation Delay Time: (Data) High-to-Low Level, $t_{PHL}$ | 5 | – | 520 | 1040 | ns |
| | 10 | – | 210 | 420 | |
| | 15 | – | 150 | 300 | |
| Low-to-High Level, $t_{PLH}$ | 5 | – | 660 | 1320 | ns |
| | 10 | – | 260 | 520 | |
| | 15 | – | 180 | 360 | |
| Propagation Delay Time: ($\overline{BL}$) High-to-Low Level, $t_{PHL}$ | 5 | – | 350 | 700 | ns |
| | 10 | – | 175 | 350 | |
| | 15 | – | 125 | 250 | |
| Low-to-High Level, $t_{PLH}$ | 5 | – | 400 | 800 | ns |
| | 10 | – | 175 | 350 | |
| | 15 | – | 150 | 300 | |
| Propagation Delay Time: ($\overline{LT}$) High-to-Low Level, $t_{PHL}$ | 5 | – | 250 | 500 | ns |
| | 10 | – | 125 | 250 | |
| | 15 | – | 85 | 170 | |
| Low-to-High Level, $t_{PLH}$ | 5 | – | 150 | 300 | ns |
| | 10 | – | 75 | 150 | |
| | 15 | – | 50 | 100 | |
| Transition Time: Low-to-High Level, $t_{TLH}$ | 5 | – | 40 | 80 | ns |
| | 10 | – | 30 | 60 | |
| | 15 | – | 25 | 50 | |
| High-to-Low Level, $t_{THL}$ | 5 | – | 125 | 310 | ns |
| | 10 | – | 75 | 185 | |
| | 15 | – | 65 | 160 | |
| Minimum Set-Up Time, $t_S$ | 5 | 150 | 75 | – | ns |
| | 10 | 70 | 35 | – | |
| | 15 | 40 | 20 | – | |
| Minimum Hold Time, $t_H$ | 5 | 0 | −75 | – | ns |
| | 10 | 0 | −35 | – | |
| | 15 | 0 | −20 | – | |
| Strobe Pulse Width, $t_W$ | 5 | 400 | 200 | – | ns |
| | 10 | 160 | 80 | – | |
| | 15 | 100 | 50 | | |
| Input Capacitance, $C_{IN}$ | | – | 5 | 7.5 | pF |

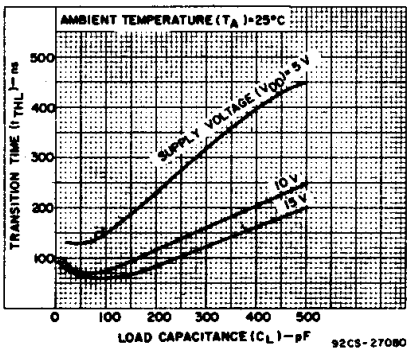



*Fig. 5 – Typical high-to-low transition time as a function of load capacitance.*

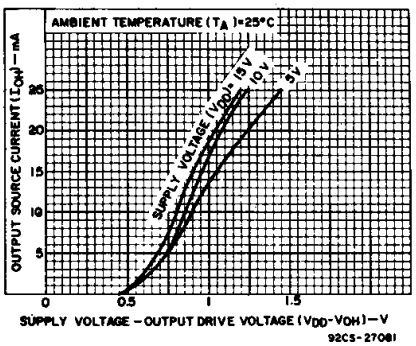



*Fig. 6 – Typical voltage drop ($V_{DD}$ to output) vs. output source current as a function of supply.*

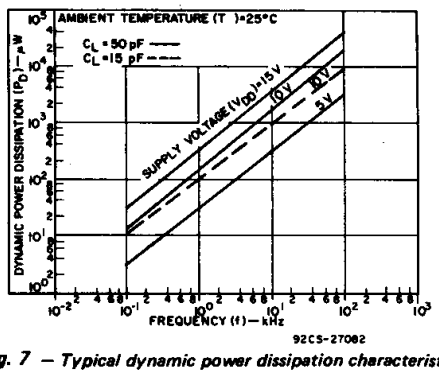



*Fig. 7 – Typical dynamic power dissipation characteristics.*

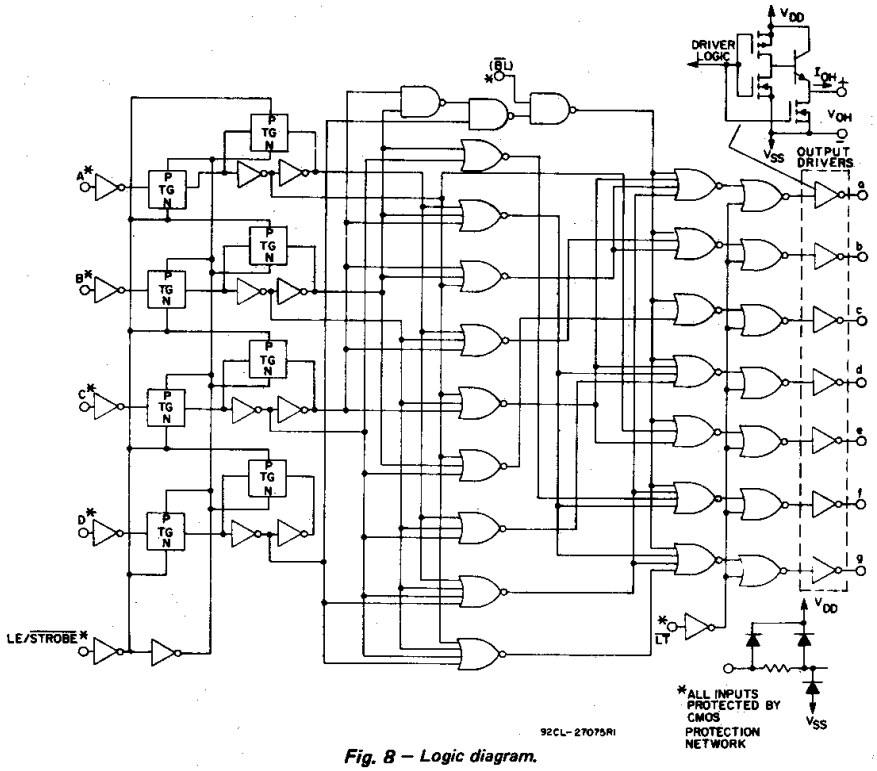



Fig. 8 – Logic diagram.

TRUTH TABLE

| LE | $\overline{BI}$ | $\overline{LT}$ | D | C | B | A | a | b | c | d | e | f | g | Display |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | 0 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| X | 0 | 1 | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 2 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 3 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 7 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 9 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | ↑ | 1 | X | X | X | X | | | | * | | | | * |

X ≡ Don't Care  * Depends on BCD code previously applied when LE = 0

Note: Display is blank for all illegal input codes (BCD > 1001).

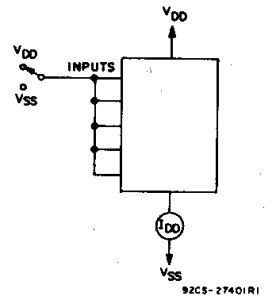



Fig. 9 – Quiescent device current.

TEST CIRCUITS

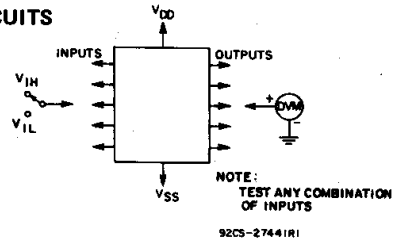



Fig. 10 – Input voltage.

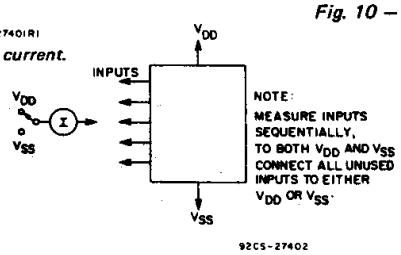
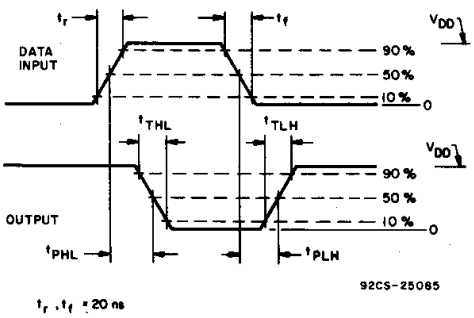



Fig.11 – Input current.




$t_r$, $t_f$ = 20 ns

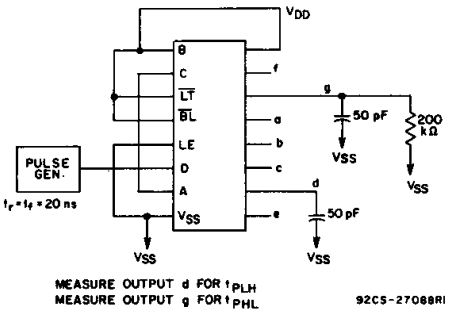



Fig.12 – Data propagation delay.

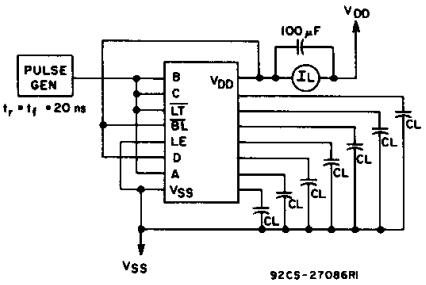
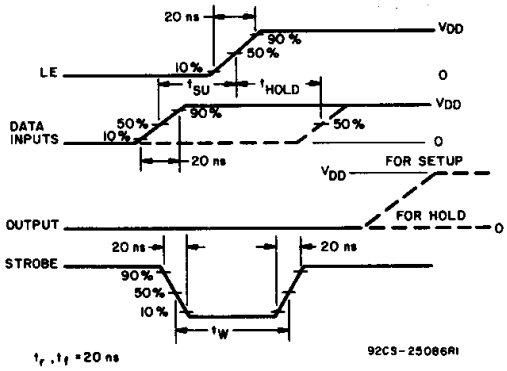



Fig. 13 – Dynamic power dissipation.

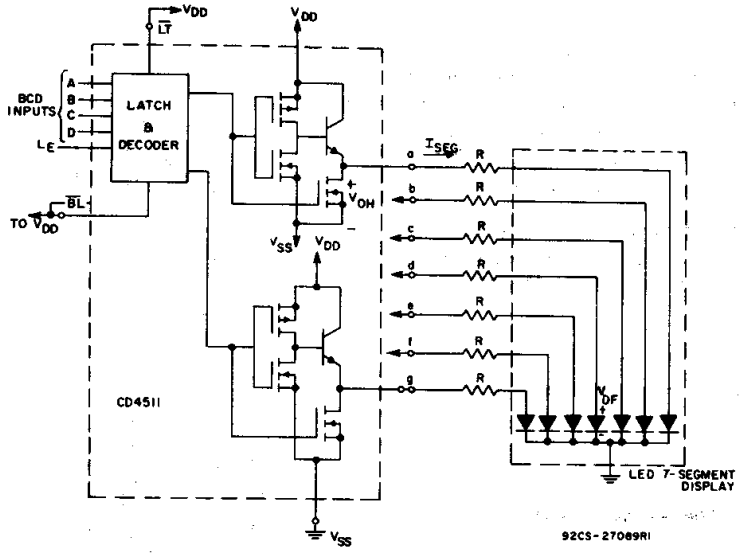



$t_r$, $t_f$ = 20 ns

Fig. 14 – Dynamic waveforms.

## APPLICATIONS

### Interfacing with Various Displays

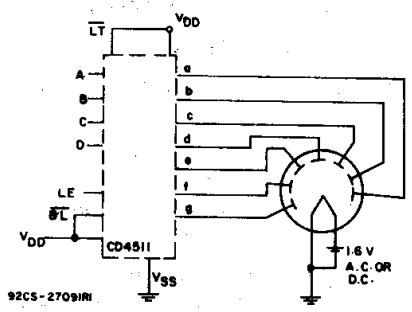



Duty Cycle = 100%

$I_{SEG} = I_{DIODE_{AVG.}}$ = 20 mA at Luminous Intensity/Segment = 250 microcandles

$$R = \frac{V_{OH} - V_{DF}}{I_{SEG}}$$

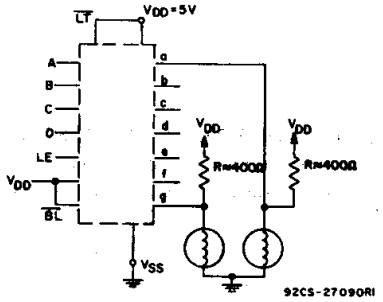
*Fig. 15 - Driving common-cathode 7-segment LED displays (example Hewlet-Packard 5082-7740).*




A medium-brightness intensity display can be obtained with low-voltage fluorescent displays such as the Tung-Sol Digivac S/G** Series.

**Trademark Tung-Sol Division Wagner Electric Co.

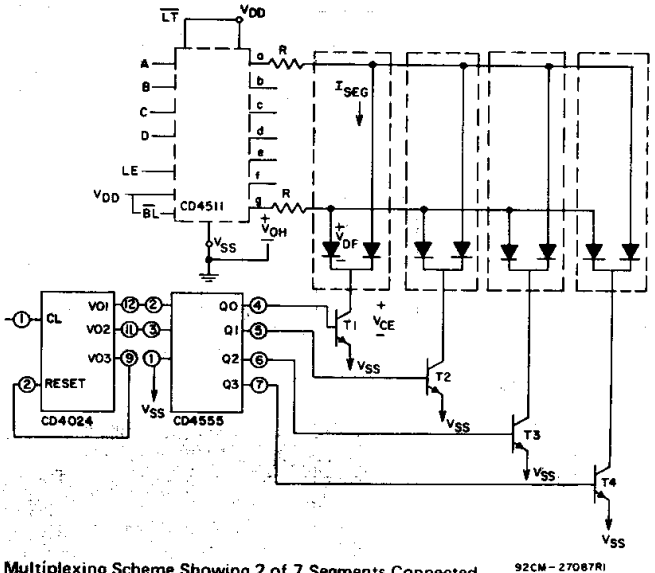
*Fig. 16 – Driving low-voltage fluorescent displays.*




2 of 7 Segments Shown Connected

Resistors R from $V_{DD}$ to each 7-segment driver output are chosen to keep all Numitron segments slightly on and warm.

*Fig. 17 – Driving incandescent displays (RCA Numitron DR2000 series displays).*




Multiplexing Scheme Showing 2 of 7 Segments Connected

Transistors $T_1$–$T_4$ (RCA-2N3053 or 2N2102) have $I_C$ Max. rating > 7x$I_{SEG}$

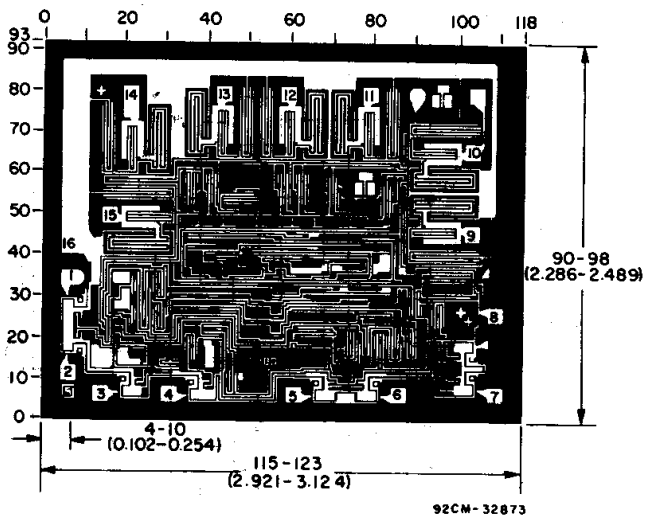
Duty Cycle = 25%

$I_{SEG} = (I_{DIODE_{AVG}}) \times 4$

$$R = \frac{(V_{OH} - V_{DF} - V_{CE})}{I_{SEG}}$$

All unused inputs on CD4555 are connected to $V_{DD}$ or $V_{SS}$.

*Fig. 18 – Multiplexing with common-cathode 7-segment LED displays (example Hewlet-Packard 5082-7404 4 character display or 4 discrete Monosanto Man 3 displays).*




*Dimensions and pad layout for CD4511B chip.*

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).*

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| CD4511BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4511BEE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4511BF | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD4511BF3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD4511BNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4511BNSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4511BPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4511BPWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4511BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4511BPWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

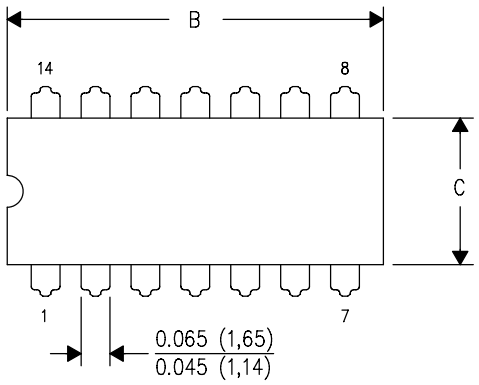
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

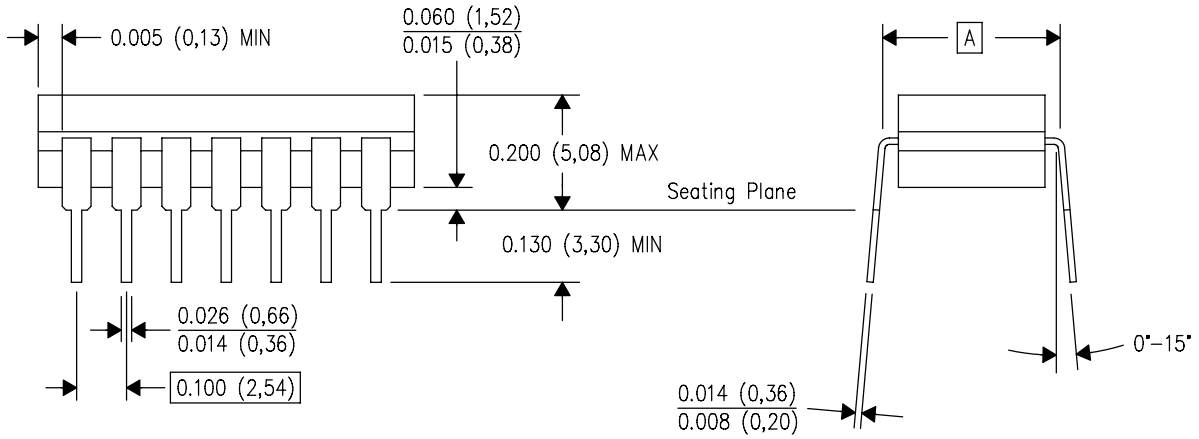
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



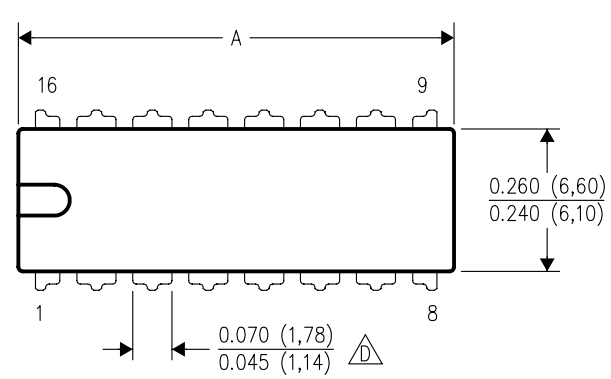

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

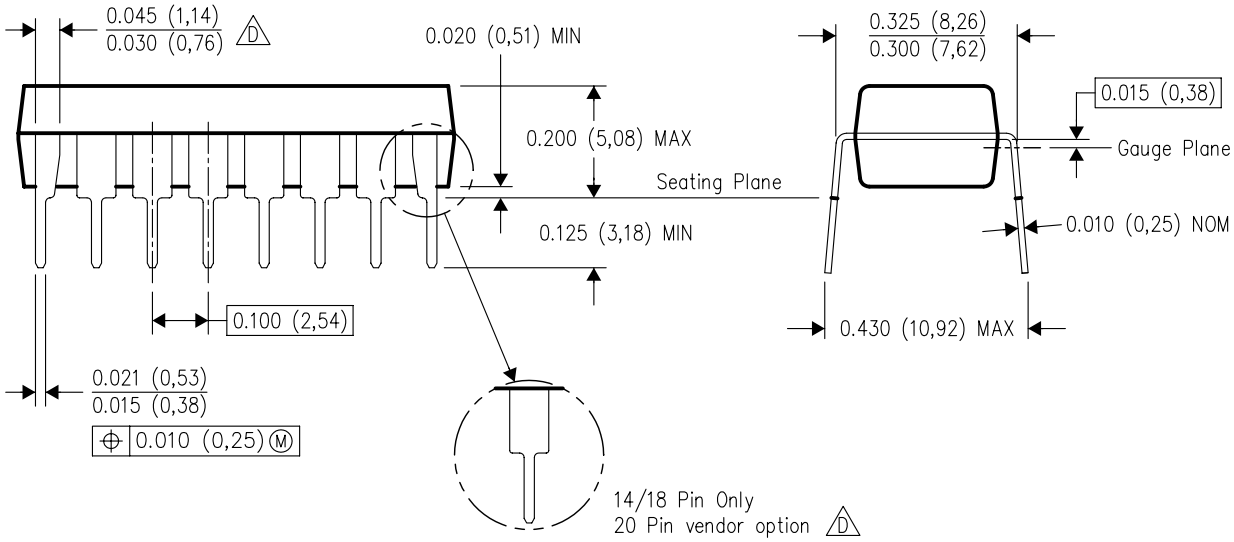
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |



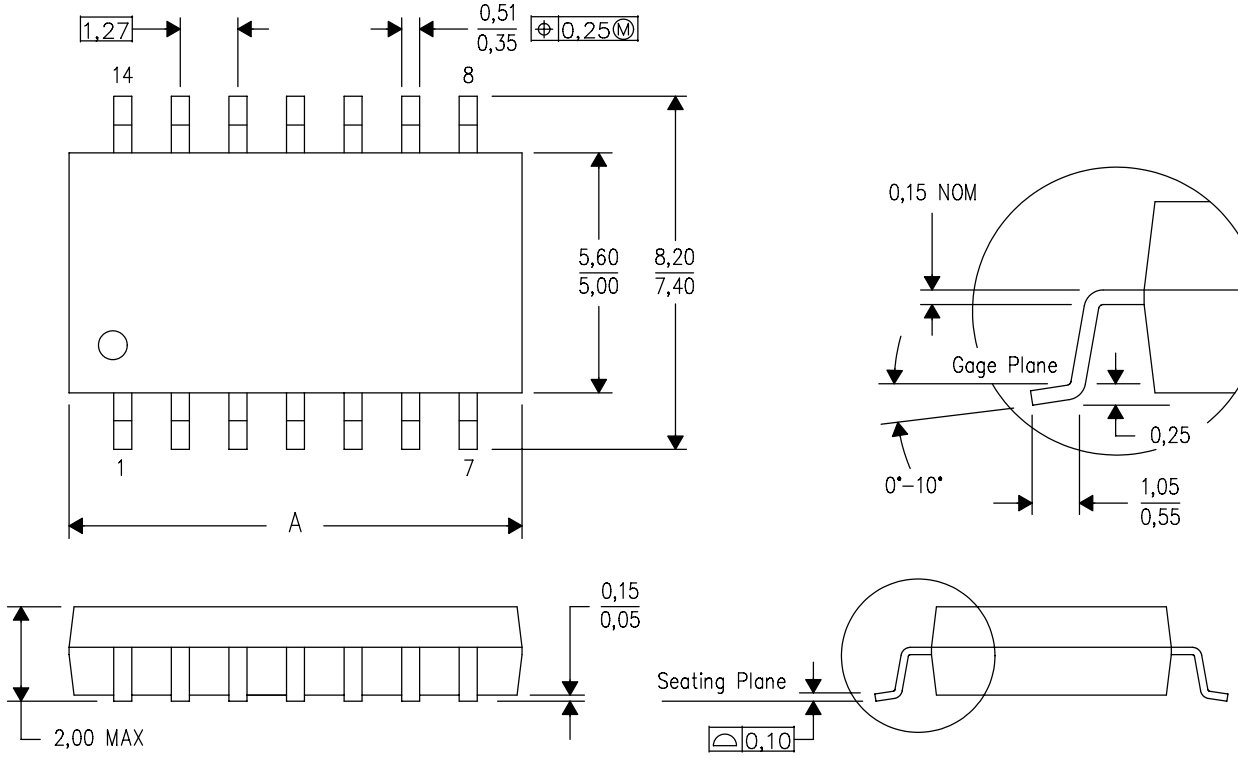

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



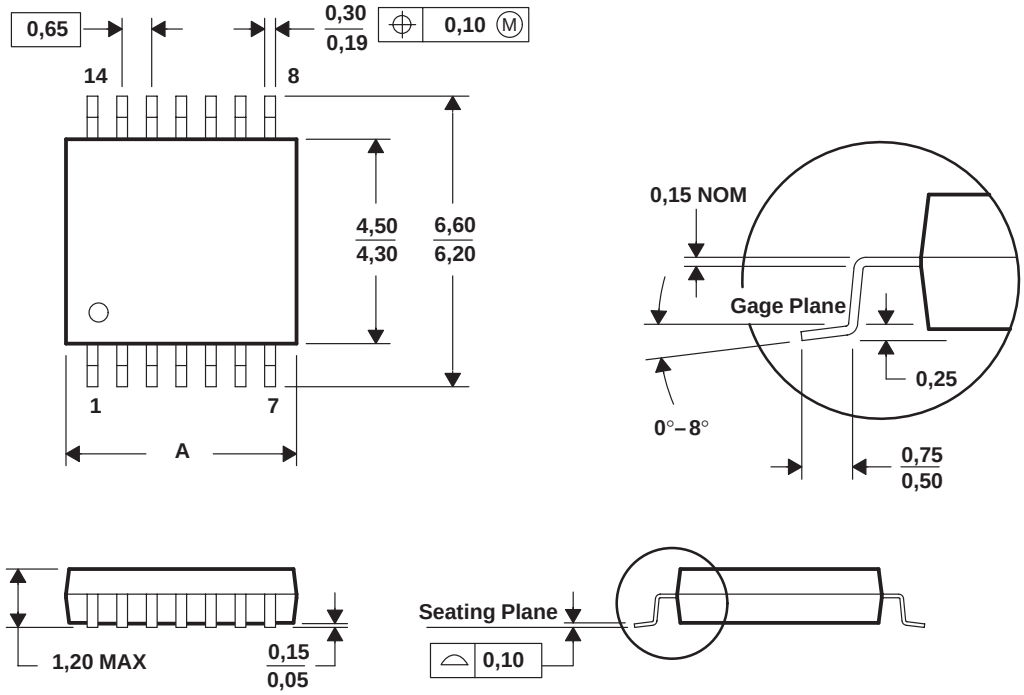

| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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