![Texas Instruments logo] **TEXAS INSTRUMENTS**

CD74HC4016

High-Speed CMOS Logic
Quad Bilateral Switch

Features

- **Wide Analog-Input-Voltage Range** . . . . **0V to 10V**
- **Low "ON" Resistance**
  - **45Ω (Typ)** . . . . **V$_{CC}$ = 4.5V**
  - **35Ω (Typ)** . . . . **V$_{CC}$ = 6V**
  - **30Ω (Typ)** . . . . **1fcV$_{CC}$ = 9V**
- **Fast Switching and Propagation Delay Times**
- **Low "OFF" Leakage Current**
- **Built-In "Break-Before-Make" Switching**
- **Suitable for Sample and Hold Applications**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **HC Types**
  - **2V to 10V Operation**
  - **High Noise Immunity: N$_{IL}$ = 30%, N$_{IH}$ = 30% of V$_{CC}$ at V$_{CC}$ = 5V**

Description

The CD74HC4016 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.
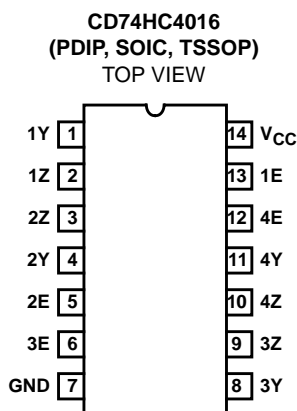
Each switch has two input/output terminals (nY, nZ) and an active high enable input (nE). Current through the switch will not cause additional V$_{CC}$ current provided the analog voltage is maintained between V$_{CC}$ and GND.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE
CD74HC4016E	-55 to 125	14 Ld PDIP
CD74HC4016M	-55 to 125	14 Ld SOIC
CD74HC4016MT	-55 to 125	14 Ld SOIC
CD74HC4016M96	-55 to 125	14 Ld SOIC
CD74HC4016PW	-55 to 125	14 Ld TSSOP
CD74HC4016PWR	-55 to 125	14 Ld TSSOP

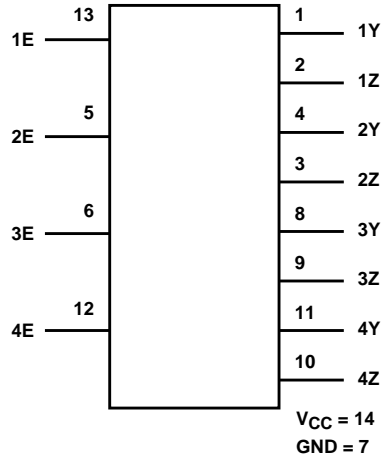NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

CD74HC4016
(PDIP, SOIC, TSSOP)
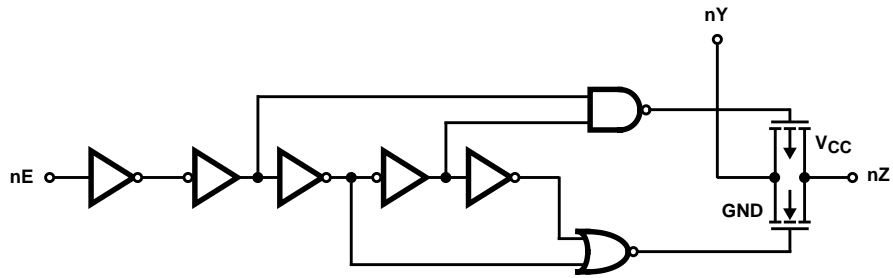TOP VIEW

1Y	1	14 V$_{CC}$
1Z	2	13 1E
2Z	3	12 4E
2Y	4	11 4Y
2E	5	10 4Z
3E	6	9 3Z
GND	7	8 3Y

Functional Diagram

13	1 → 1Y
1E	2 → 1Z
5	4 → 2Y
2E	3 → 2Z
6	8 → 3Y
3E	9 → 3Z
12	11 → 4Y
4E	10 → 4Z

V_{CC} = 14
GND = 7

TRUTH TABLE

INPUT nE	SWITCH
L	OFF
H	ON

H = High Level Voltage
L = Low Level Voltage

Logic Diagram

CD74HC4016

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
   For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . ±20mA
DC Drain Current, per Output, I_O
   For -0.5V < V_O < V_{CC} + 0.5V . . . . ±25mA
DC Output Diode Current, I_{OK}
   For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
   For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
   HC Types . . . . .2V to 10V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
   2V . . . . 1000ns (Max)
   4.5V . . . . 500ns (Max)
   6V . . . . 400ns (Max)
   9V . . . . 250ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
E (PDIP) Package	80
M (SOIC) Package.	86
PW (TSSOP) Package	96

Maximum Junction Temperature (Plastic Package) . . . . 150°C
Maximum Storage Temperature Range . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implie

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	V_{IS} (V)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
"ON" Resistance I_O = 1mA	R_{ON}	V_{IH} or V_{IL}	V_{CC} or GND	4.5	-	45	180	-	225	-	270	Ω
				6	-	35	160	-	200	-	240	Ω
				9	-	30	135	-	170	-	205	Ω
				4.5	-	85	320	-	400	-	480	Ω
				6	-	55	240	-	300	-	360	Ω
				9	-	35	170	-	215	-	255	Ω
Maximum "ON" Resistance Between Any Two Switches	ΔR_{ON}	V_{IL} or V_{IH}	V_{CC} or GND	4.5	-	10	-	-	-	-	-	Ω
				6	-	8.5	-	-	-	-	-	Ω
Switch Off Leakage Current	I_{IZ}	En = GND	V_{CC} or GND	6	-	-	±0.1	-	±1	-	±1	µA
				10	-	-	±0.1	-	±1	-	±1	µA
Logic Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	V_{IS} (V)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current I_O = 0mA	I_{CC}	V_{CC} or GND	V_{CC} or GND	6	-	-	2	-	20	-	40	µA
				10	-	-	16	-	160	-	320	µA

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay, Switch In to Switch Out	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
		C_L = 15pF	5	-	4	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	10	-	13	-	15	ns
			9	-	-	8	-	10	-	12	ns
Propagation Delay, Switch Turn-On En to Out	t_{PZH}, t_{PZL}	C_L = 50pF	2	-	-	190	-	240	-	285	ns
			4.5	-	-	38	-	48	-	57	ns
		C_L = 15pF	5	-	16	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	32	-	41	-	48	ns
			9	-	-	28	-	35	-	42	ns
Propagation Delay, Switch Turn-Off En to Out	t_{PHZ}, t_{PLZ}	C_L = 50pF	2	-	-	145	-	180	-	220	ns
			4.5	-	-	29	-	36	-	44	ns
		C_L = 15pF	5	-	12	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	25	-	31	-	38	ns
			9	-	-	22	-	28	-	33	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 2, 3)	C_{PD}	-	5	-	12	-	-	-	-	-	pF

NOTES:

2. C_{PD} is used to determine the dynamic power consumption, per package.

3. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, C_S = switch capacitance, V_{CC} = supply voltage.

Analog Channel Specifications T_A = 25°C

PARAMETER	TEST CONDITIONS	V_{CC} (V)	CD74HC4016	UNITS
Switch Frequency Response Bandwidth at -3dB Figure 3	Figure 6, Notes 4, 5	4.5	>200	MHz
Crosstalk Between Any Two Switches, Figure 4	Figure 5, Notes 5, 6	4.5	TBE	dB
Total Harmonic Distortion	1kHz, V_{IS} = 4V_{P-P} Figure 7	4, 5	0.078	%
	1kHz, V_{IS} = 8V_{P-P} Figure 7	9	0.018	%

Analog Channel Specifications $T_A = 25^oC$ (Continued)

PARAMETER	TEST CONDITIONS	V_{CC} (V)	CD74HC4016	UNITS
Control to Switch Feedthrough Noise	Figure 8	4.5	TBE	mV
		9	TBE	mV
Switch "OFF" Signal Feedthrough, Figure 4	Figure 9, Notes 5, 6	4.5	-62	dB
Switch Input Capacitance, C_S		-	5	pF

NOTES:

4. Adjust input level for 0dBm at output, f = 1MHz.

5. V_{IS} is centered at $V_{CC}/2$.

6. Adjust input for 0dBm at V_{IS}.

Typical Performance Curves
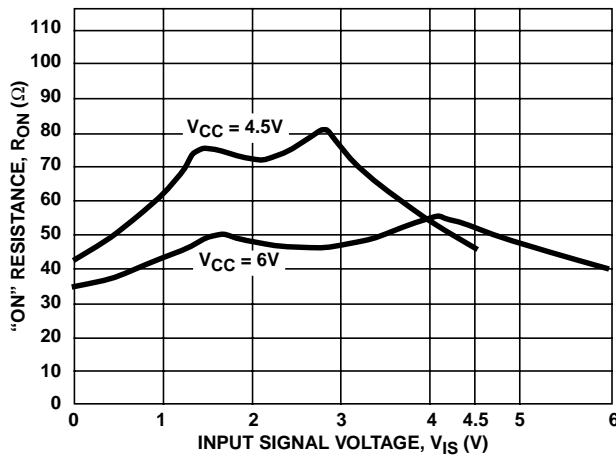
FIGURE 1. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE
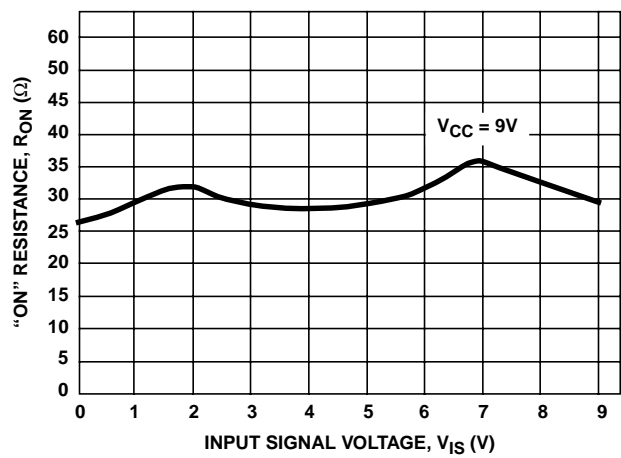
FIGURE 2. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE
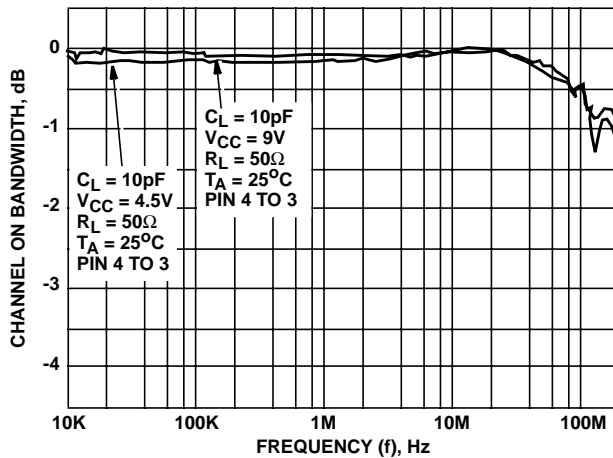
FIGURE 3. SWITCH FREQUENCY RESPONSE
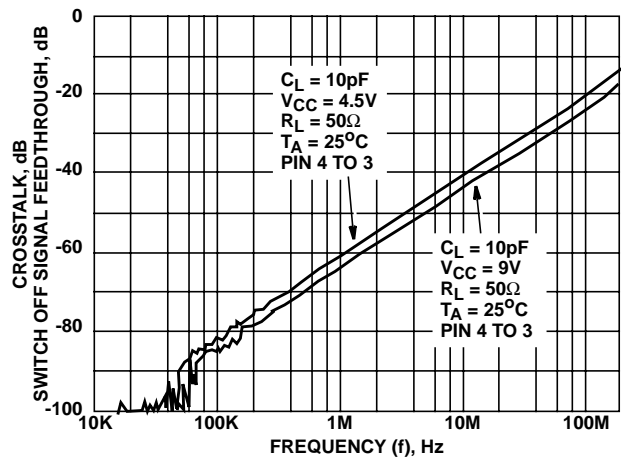
FIGURE 4. SWITCH-OFF SIGNAL FEEDTHROUGH AND CROSSTALK vs FREQUENCY
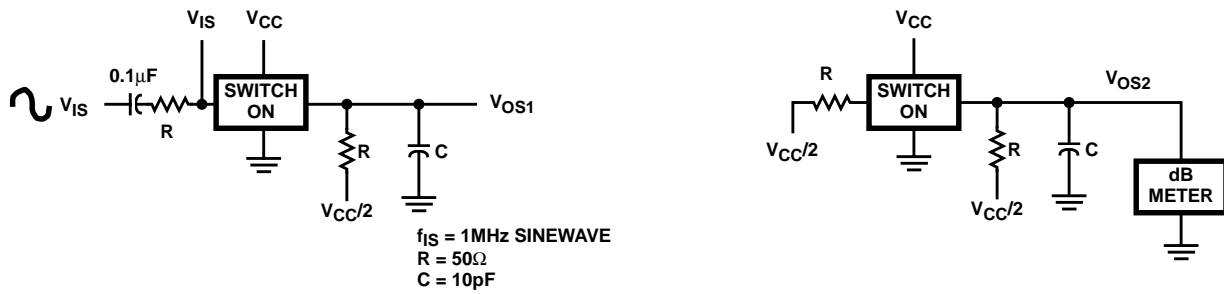
Analog Test Circuits

f_{IS} = 1MHz SINEWAVE
R = 50Ω
C = 10pF

FIGURE 5. CROSSTALK BETWEEN TWO SWITCHES TEST CIRCUIT
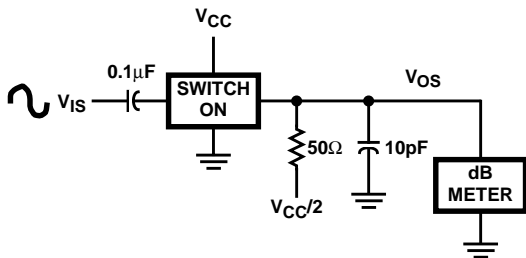
FIGURE 6. FREQUENCY RESPONSE TEST CIRCUIT

f_{IS} = 1kHz TO 10kHz
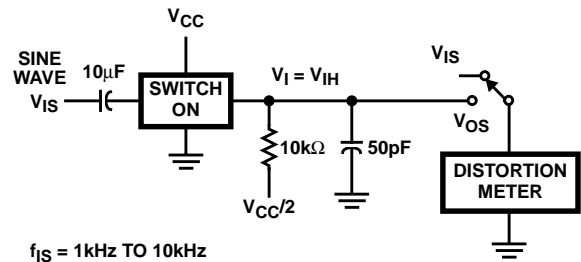
FIGURE 7. TOTAL HARMONIC DISTORTION TEST CIRCUIT
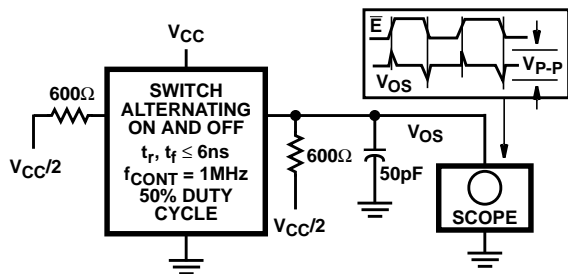
FIGURE 8. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

$f_{IS} \geq$ 1MHz SINEWAVE
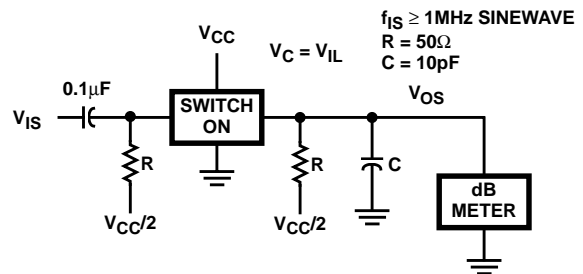R = 50Ω
C = 10pF

FIGURE 9. SWITCH OFF SIGNAL FEEDTHROUGH

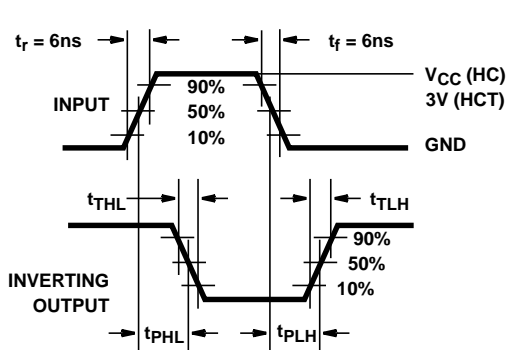## *Test Circuits and Waveforms*

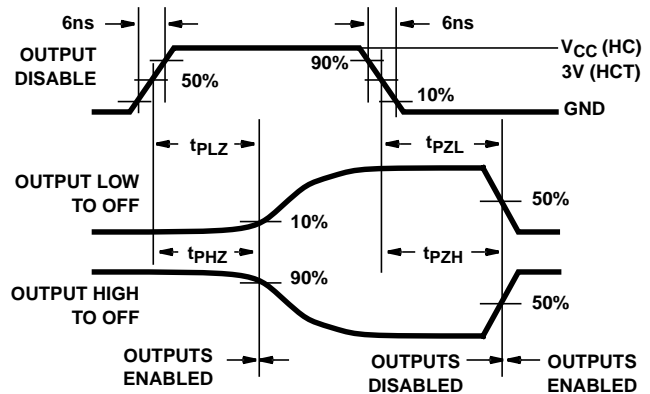**FIGURE 10. HC/HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

FIGURE 11. SWITCH TURN-ON AND TURN-OFF PROPAGATION DELAY TIMES

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CD74HC4016E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC4016EE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC4016M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4016M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4016MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4016MTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4016PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4016PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4016PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4016PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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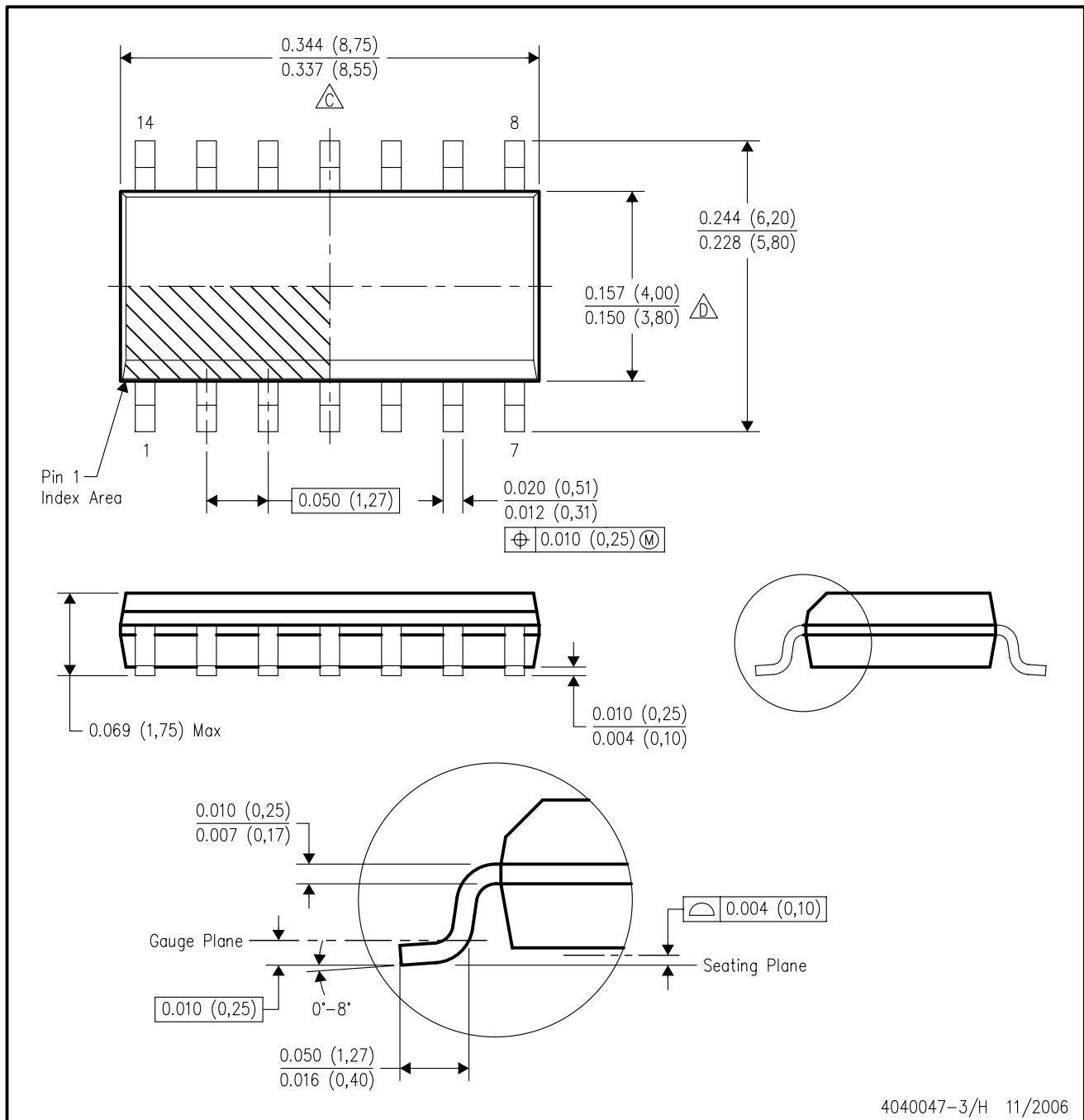N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) ⚠D

0.045 (1,14) / 0.030 (0,76) ⚠D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option ⚠D

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
⚠C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
⚠D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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D (R−PDSO−G14) PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)
⟋C⟍

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⟋D⟍

1   7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/H 11/2006

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
    ⟋C⟍ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
          not exceed .006 (0,15) per end.
    ⟋D⟍ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
         E. Reference JEDEC MS−012 variation AB.

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PW (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

0,65

0,30 / 0,19

⊕ 0,10 Ⓜ

14 8

1 7

4,50 / 4,30

6,60 / 6,20

A

0,15 NOM

Gage Plane

0°−8°

0,25

0,75 / 0,50

1,20 MAX

0,15 / 0,05

Seating Plane

△ 0,10

DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
     B. This drawing is subject to change without notice.
     C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
     D. Falls within JEDEC MO-153

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