



MICROCHIP

PIC16F84A

18-pin *Enhanced* Flash/EEPROM 8-Bit Microcontroller

Devices Included in this Data Sheet:

- PIC16F84A
- Extended voltage range device available (PIC16LF84A)

High Performance RISC CPU Features:

- Only 35 single word instructions to learn
- All instructions single cycle except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
DC - 200 ns instruction cycle
- 1024 words of program memory
- 68 bytes of data RAM
- 64 bytes of data EEPROM
- 14-bit wide instruction words
- 8-bit wide data bytes
- 15 special function hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources:
 - External RB0/INT pin
 - TMR0 timer overflow
 - PORTB<7:4> interrupt on change
 - Data EEPROM write complete

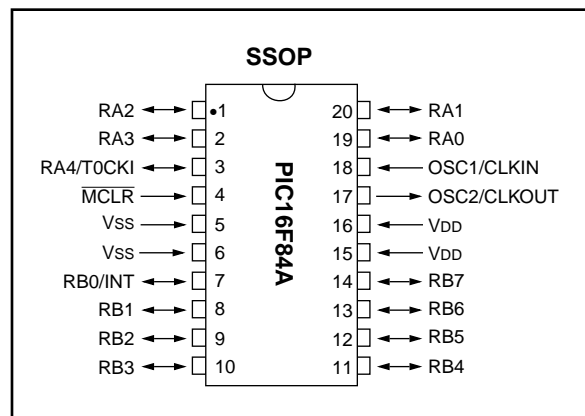
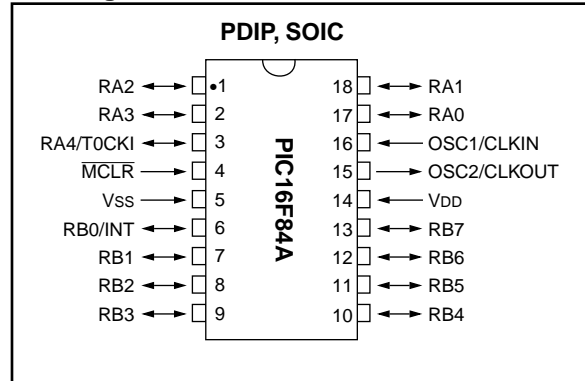
Peripheral Features:

- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
 - 25 mA sink max. per pin
 - 25 mA source max. per pin
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler

Special Microcontroller Features:

- 1000 erase/write cycles *Enhanced* Flash program memory
- 1,000,000 typical erase/write cycles EEPROM data memory
- EEPROM Data Retention > 40 years
- In-Circuit Serial Programming (ICSP™) - via two pins
- Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Code-protection
- Power saving SLEEP mode
- Selectable oscillator options

Pin Diagrams



CMOS *Enhanced* Flash/EEPROM Technology:

- Low-power, high-speed technology
- Fully static design
- Wide operating voltage range:
 - Commercial: 2.0V to 5.5V
 - Industrial: 2.0V to 5.5V
- Low power consumption:
 - < 2 mA typical @ 5V, 4 MHz
 - 15 µA typical @ 2V, 32 kHz
 - < 0.5 µA typical standby current @ 2V

PIC16F84A

Table of Contents

1.0 Device Overview	3
2.0 Memory Organization	5
3.0 I/O Ports	13
4.0 Timer0 Module	17
5.0 Data EEPROM Memory	19
6.0 Special Features of the CPU	21
7.0 Instruction Set Summary	33
8.0 Development Support	35
9.0 Electrical Characteristics for PIC16F84A	41
10.0 DC & AC Characteristics Graphs/Tables	53
11.0 Packaging Information	55
Appendix A: Revision History	59
Appendix B: Conversion Considerations	59
Appendix C: Migration from Baseline to Midrange Devices	62
Index	63
On-Line Support	65
Reader Response	66
PIC16F84A Product Identification System	67

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Errata

An errata sheet may exist for current devices, describing minor operational differences (from the data sheet) and recommended workarounds. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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Corrections to this Data Sheet

We constantly strive to improve the quality of all our products and documentation. We have spent a great deal of time to ensure that this document is correct. However, we realize that we may have missed a few things. If you find any information that is missing or appears in error, please:

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- E-mail us at webmaster@microchip.com.

We appreciate your assistance in making this a better document.

1.0 DEVICE OVERVIEW

This document contains device-specific information for the operation of the PIC16F84A device. Additional information may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023), which may be downloaded from the Microchip website. The Reference Manual should be considered a complementary document to this data sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

The PIC16F84A belongs to the mid-range family of the PICmicro™ microcontroller devices. A block diagram of the device is shown in Figure 1-1.

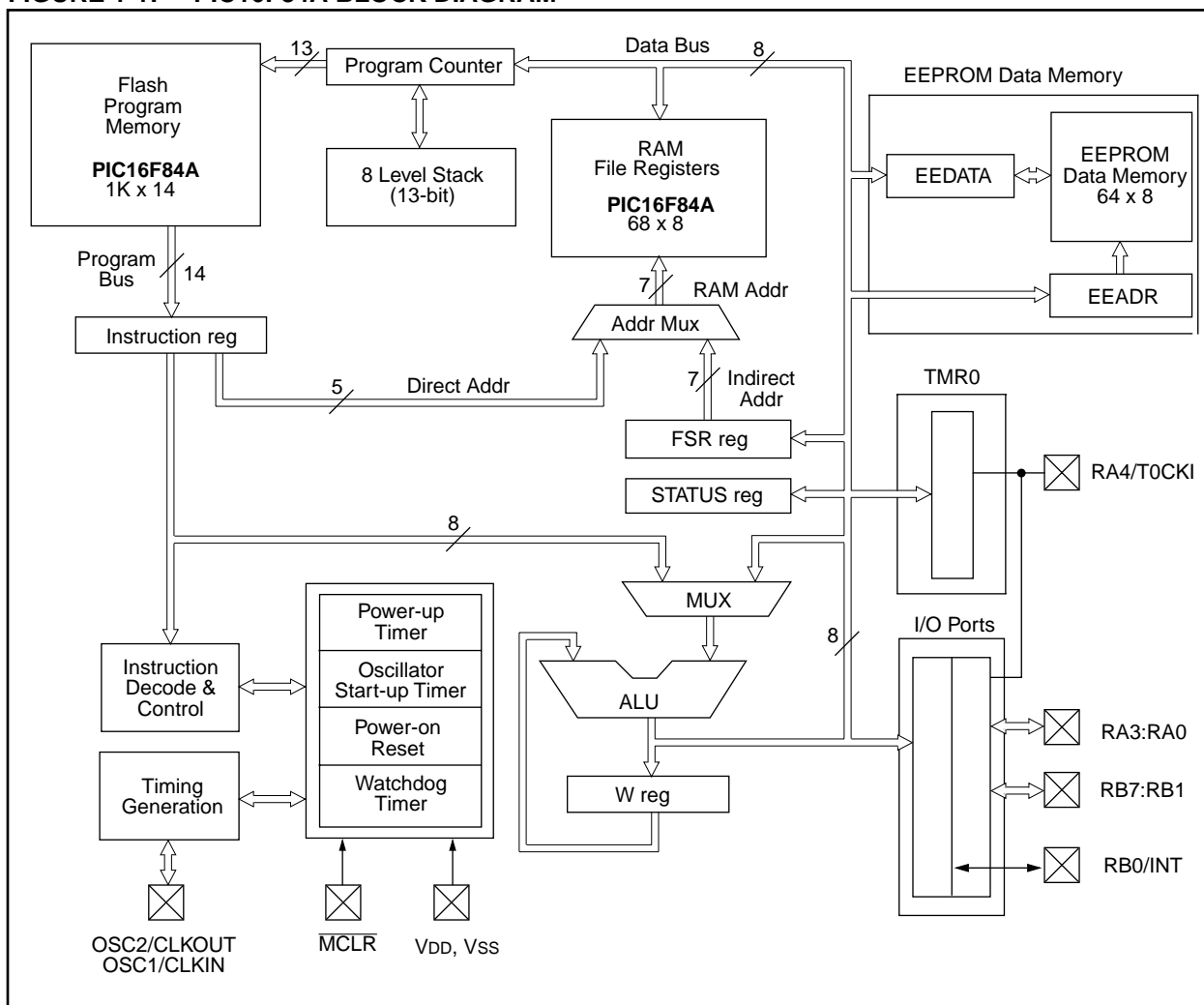
The program memory contains 1K words, which translates to 1024 instructions, since each 14-bit program memory word is the same width as each device instruction. The data memory (RAM) contains 68 bytes. Data EEPROM is 64 bytes.

There are also 13 I/O pins that are user-configured on a pin-to-pin basis. Some pins are multiplexed with other device functions. These functions include:

- External interrupt
- Change on PORTB interrupt
- Timer0 clock input

Table 1-1 details the pinout of the device with descriptions and details for each pin.

FIGURE 1-1: PIC16F84A BLOCK DIAGRAM



PIC16F84A

TABLE 1-1 PIC16F84A PINOUT DESCRIPTION

Pin Name	DIP No.	SOIC No.	SSOP No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	16	18	I	ST/CMOS ⁽³⁾	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	19	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR	4	4	4	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
RA0	17	17	19	I/O	TTL	<p>PORTA is a bi-directional I/O port.</p> <p>Can also be selected to be the clock input to the TMR0 timer/counter. Output is open drain type.</p>
RA1	18	18	20	I/O	TTL	
RA2	1	1	1	I/O	TTL	
RA3	2	2	2	I/O	TTL	
RA4/T0CKI	3	3	3	I/O	ST	
RB0/INT	6	6	7	I/O	TTL/ST ⁽¹⁾	<p>PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.</p> <p>RB0/INT can also be selected as an external interrupt pin.</p> <p>Interrupt on change pin.</p> <p>Interrupt on change pin.</p> <p>Interrupt on change pin. Serial programming clock.</p> <p>Interrupt on change pin. Serial programming data.</p>
RB1	7	7	8	I/O	TTL	
RB2	8	8	9	I/O	TTL	
RB3	9	9	10	I/O	TTL	
RB4	10	10	11	I/O	TTL	
RB5	11	11	12	I/O	TTL	
RB6	12	12	13	I/O	TTL/ST ⁽²⁾	
RB7	13	13	14	I/O	TTL/ST ⁽²⁾	
Vss	5	5	5,6	P	—	Ground reference for logic and I/O pins.
VDD	14	14	15,16	P	—	Positive supply for logic and I/O pins.

Legend: I= input O = output I/O = Input/Output P = power
 — = Not used TTL = TTL input ST = Schmitt Trigger input

- Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
 2: This buffer is a Schmitt Trigger input when used in serial programming mode.
 3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

2.0 MEMORY ORGANIZATION

There are two memory blocks in the PIC16F84A. These are the program memory and the data memory. Each block has its own bus, so that access to each block can occur during the same oscillator cycle.

The data memory can further be broken down into the general purpose RAM and the Special Function Registers (SFRs). The operation of the SFRs that control the "core" are described here. The SFRs used to control the peripheral modules are described in the section discussing each individual peripheral module.

The data memory area also contains the data EEPROM memory. This memory is not directly mapped into the data memory, but is indirectly mapped. That is, an indirect address pointer specifies the address of the data EEPROM memory to read/write. The 64 bytes of data EEPROM memory have the address range 0h-3Fh. More details on the EEPROM memory can be found in Section 5.0.

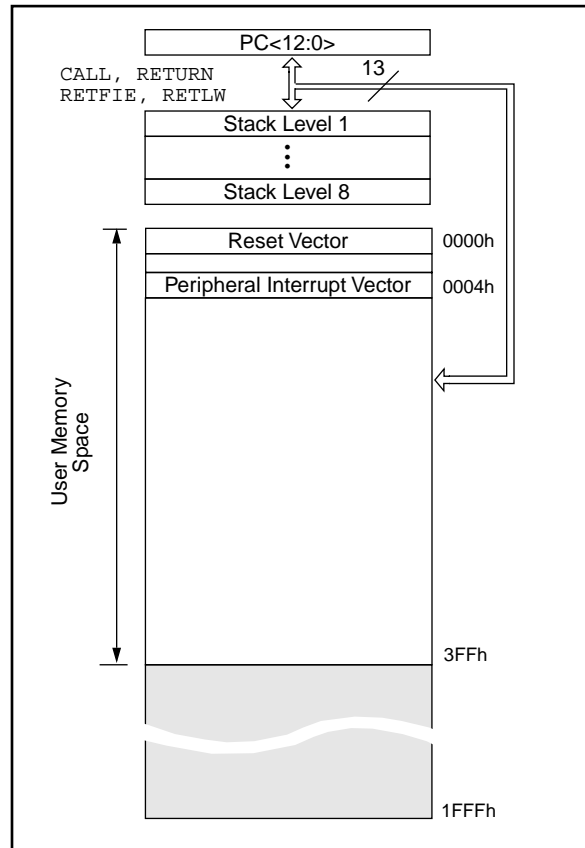
Additional information on device memory may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023).

2.1 Program Memory Organization

The PIC16FXX has a 13-bit program counter capable of addressing an 8K x 14 program memory space. For the PIC16F84A, the first 1K x 14 (0000h-03FFh) are physically implemented (Figure 2-1). Accessing a location above the physically implemented address will cause a wraparound. For example, for locations 20h, 420h, 820h, C20h, 1020h, 1420h, 1820h, and 1C20h will be the same instruction.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK - PIC16F84A



PIC16F84A

2.2 Data Memory Organization

The data memory is partitioned into two areas. The first is the Special Function Registers (SFR) area, while the second is the General Purpose Registers (GPR) area. The SFRs control the operation of the device.

Portions of data memory are banked. This is for both the SFR area and the GPR area. The GPR area is banked to allow greater than 116 bytes of general purpose RAM. The banked areas of the SFR are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the STATUS Register. Figure 2-1 shows the data memory map organization.

Instructions *MOVWF* and *MOVF* can move values from the W register to any location in the register file ("F"), and vice-versa.

The entire data memory can be accessed either directly using the absolute address of each register file or indirectly through the File Select Register (FSR) (Section 2.4). Indirect addressing uses the present value of the RP0 bit for access into the banked areas of data memory.

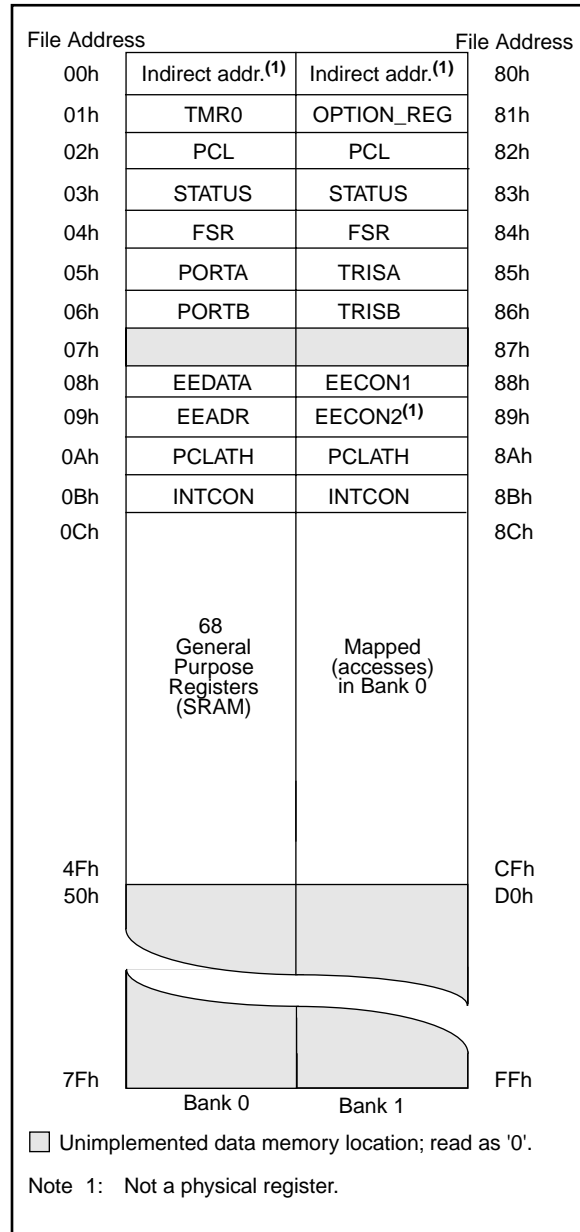
Data memory is partitioned into two banks which contain the general purpose registers and the special function registers. Bank 0 is selected by clearing the RP0 bit (STATUS<5>). Setting the RP0 bit selects Bank 1. Each Bank extends up to 7Fh (128 bytes). The first twelve locations of each Bank are reserved for the Special Function Registers. The remainder are General Purpose Registers implemented as static RAM.

2.2.1 GENERAL PURPOSE REGISTER FILE

Each General Purpose Register (GPR) is 8 bits wide and is accessed either directly or indirectly through the FSR (Section 2.4).

The GPR addresses in bank 1 are mapped to addresses in bank 0. As an example, addressing location 0Ch or 8Ch will access the same GPR.

FIGURE 2-1: REGISTER FILE MAP - PIC16F84A



2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (Figure 2-1 and Table 2-1) are used by the CPU and Peripheral functions to control the device operation. These registers are static RAM.

The special function registers can be classified into two sets, core and peripheral. Those associated with the core functions are described in this section. Those related to the operation of the peripheral features are described in the section for that specific feature.

TABLE 2-1 REGISTER FILE SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note3)		
Bank 0													
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								----	----		
01h	TMR0	8-bit real-time clock/counter								xxxx	xxxx	uuuu	uuuu
02h	PCL	Low order 8 bits of the Program Counter (PC)								0000	0000	0000	0000
03h	STATUS ⁽²⁾	IRP	RP1	RP0	\overline{TO}	\overline{PD}	Z	DC	C	0001	1xxx	000q	quuu
04h	FSR	Indirect data memory address pointer 0								xxxx	xxxx	uuuu	uuuu
05h	PORTA ⁽⁴⁾	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x	xxxx	---u	uuuu
06h	PORTB ⁽⁵⁾	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx	xxxx	uuuu	uuuu
07h		Unimplemented location, read as '0'								----	----	----	----
08h	EEDATA	EEPROM data register								xxxx	xxxx	uuuu	uuuu
09h	EEADR	EEPROM address register								xxxx	xxxx	uuuu	uuuu
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC ⁽¹⁾					---	0000	---	0000
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000	000x	0000	000u
Bank 1													
80h	INDF	Uses contents of FSR to address data memory (not a physical register)								----	----	----	----
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111	1111	1111	1111
82h	PCL	Low order 8 bits of Program Counter (PC)								0000	0000	0000	0000
83h	STATUS ⁽²⁾	IRP	RP1	RP0	\overline{TO}	\overline{PD}	Z	DC	C	0001	1xxx	000q	quuu
84h	FSR	Indirect data memory address pointer 0								xxxx	xxxx	uuuu	uuuu
85h	TRISA	—	—	—	PORTA data direction register					---	1111	---	1111
86h	TRISB	PORTB data direction register								1111	1111	1111	1111
87h		Unimplemented location, read as '0'								----	----	----	----
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---	x000	---	q000
89h	EECON2	EEPROM control register 2 (not a physical register)								----	----	----	----
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC ⁽¹⁾					---	0000	---	0000
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000	000x	0000	000u

Legend: x = unknown, u = unchanged. - = unimplemented read as '0', q = value depends on condition.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a slave register for PC<12:8>. The contents of PCLATH can be transferred to the upper byte of the program counter, but the contents of PC<12:8> is never transferred to PCLATH.

- 2: The \overline{TO} and \overline{PD} status bits in the STATUS register are not affected by a \overline{MCLR} reset.
- 3: Other (non power-up) resets include: external reset through \overline{MCLR} and the Watchdog Timer Reset.
- 4: On any device reset, these pins are configured as inputs.
- 5: This is the value that will be in the port output latch.

PIC16F84A

2.2.2.1 STATUS REGISTER

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bit for data memory.

As with any register, the STATUS register can be the destination for any instruction. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to device logic. Furthermore, the \overline{TO} and \overline{PD} bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

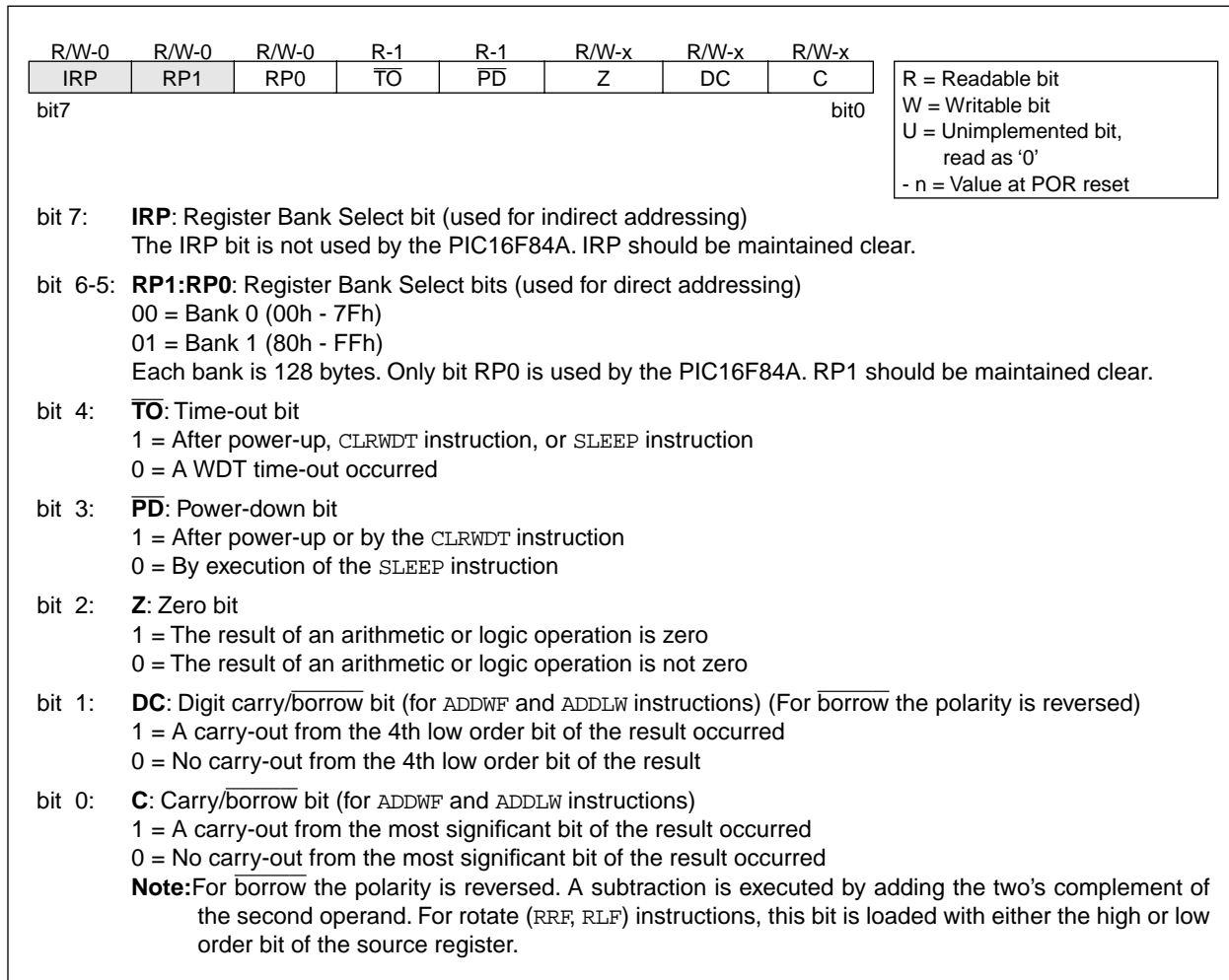
Only the `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions should be used to alter the STATUS register (Table 7-2) because these instructions do not affect any status bit.

Note 1: The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16F84A and should be programmed as cleared. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

Note 2: The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

Note 3: When the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. The specified bit(s) will be updated according to device logic

FIGURE 2-1: STATUS REGISTER (ADDRESS 03h, 83h)



2.2.2.2 OPTION_REG REGISTER

The OPTION_REG register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external INT interrupt, TMR0, and the weak pull-ups on PORTB.

Note: When the prescaler is assigned to the WDT (PSA = '1'), TMR0 has a 1:1 prescaler assignment.

FIGURE 2-1: OPTION_REG REGISTER (ADDRESS 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPŪ	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
							bit0
bit7							

R = Readable bit
 W = Writable bit
 U = Unimplemented bit, read as '0'
 - n = Value at POR reset

bit 7: **RBPŪ**: PORTB Pull-up Enable bit
 1 = PORTB pull-ups are disabled
 0 = PORTB pull-ups are enabled (by individual port latch values)

bit 6: **INTEDG**: Interrupt Edge Select bit
 1 = Interrupt on rising edge of RB0/INT pin
 0 = Interrupt on falling edge of RB0/INT pin

bit 5: **T0CS**: TMR0 Clock Source Select bit
 1 = Transition on RA4/T0CKI pin
 0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit
 1 = Increment on high-to-low transition on RA4/T0CKI pin
 0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
 1 = Prescaler assigned to the WDT
 0 = Prescaler assigned to TMR0

bit 2-0: **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

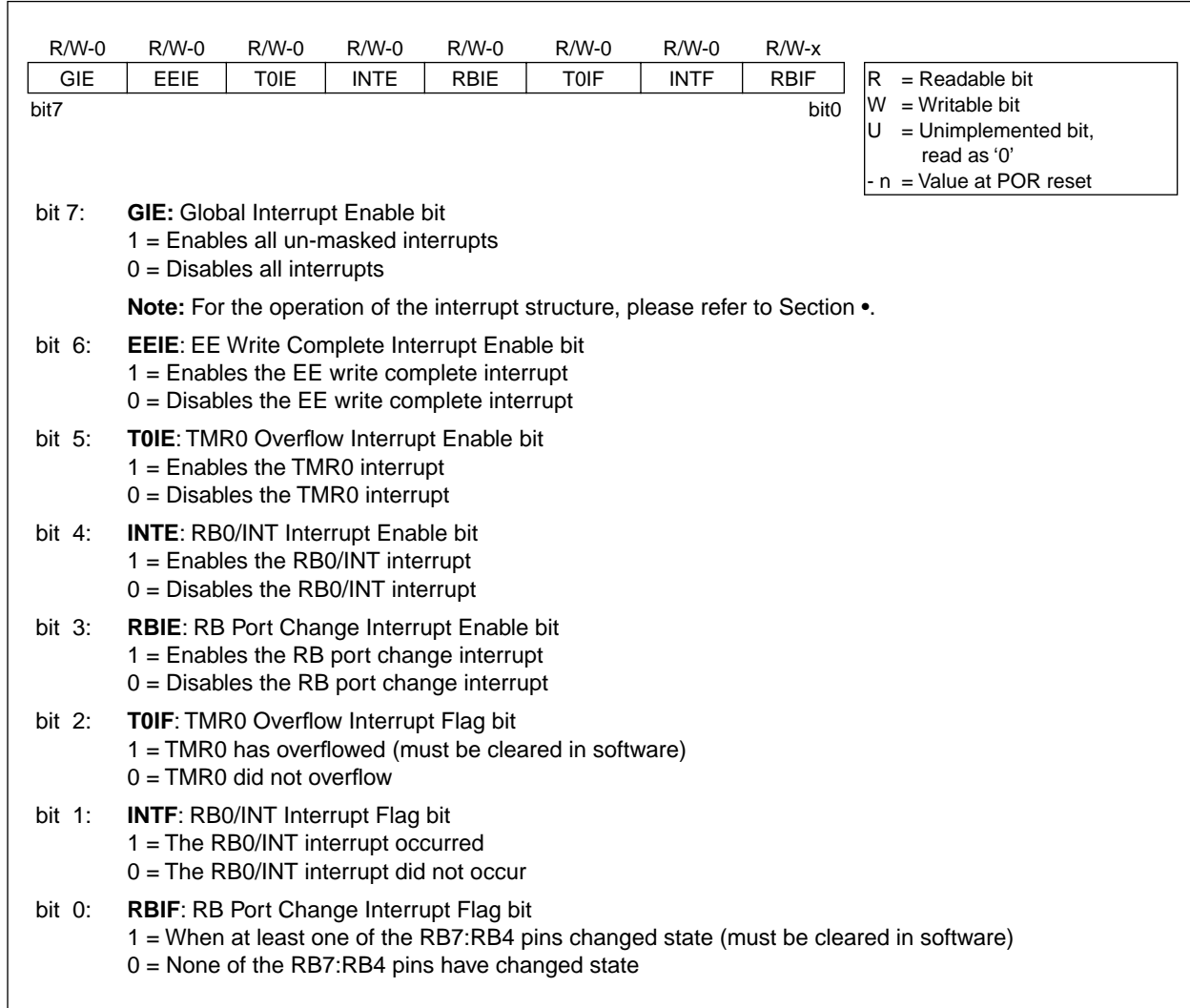
PIC16F84A

2.2.2.3 INTCON REGISTER

The INTCON register is a readable and writable register which contains the various enable bits for all interrupt sources.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 2-1: INTCON REGISTER (ADDRESS 0Bh, 8Bh)



2.3 PCL and PCLATH

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 13 bits wide. The low byte is called the PCL register. This register is readable and writable. The high byte is called the PCH register. This register contains the PC<12:8> bits and is not directly readable or writable. All updates to the PCH register go through the PCLATH register.

2.3.1 STACK

The stack allows a combination of up to 8 program calls and interrupts to occur. The stack contains the return address from this branch in program execution.

Midrange devices have an 8 level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not modified when the stack is PUSHed or POPed.

After the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

2.4 Indirect Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 2-1: INDIRECT ADDRESSING

- Register file 05 contains the value 10h
- Register file 06 contains the value 0Ah
- Load the value 05 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 06)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 2-2.

EXAMPLE 2-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```

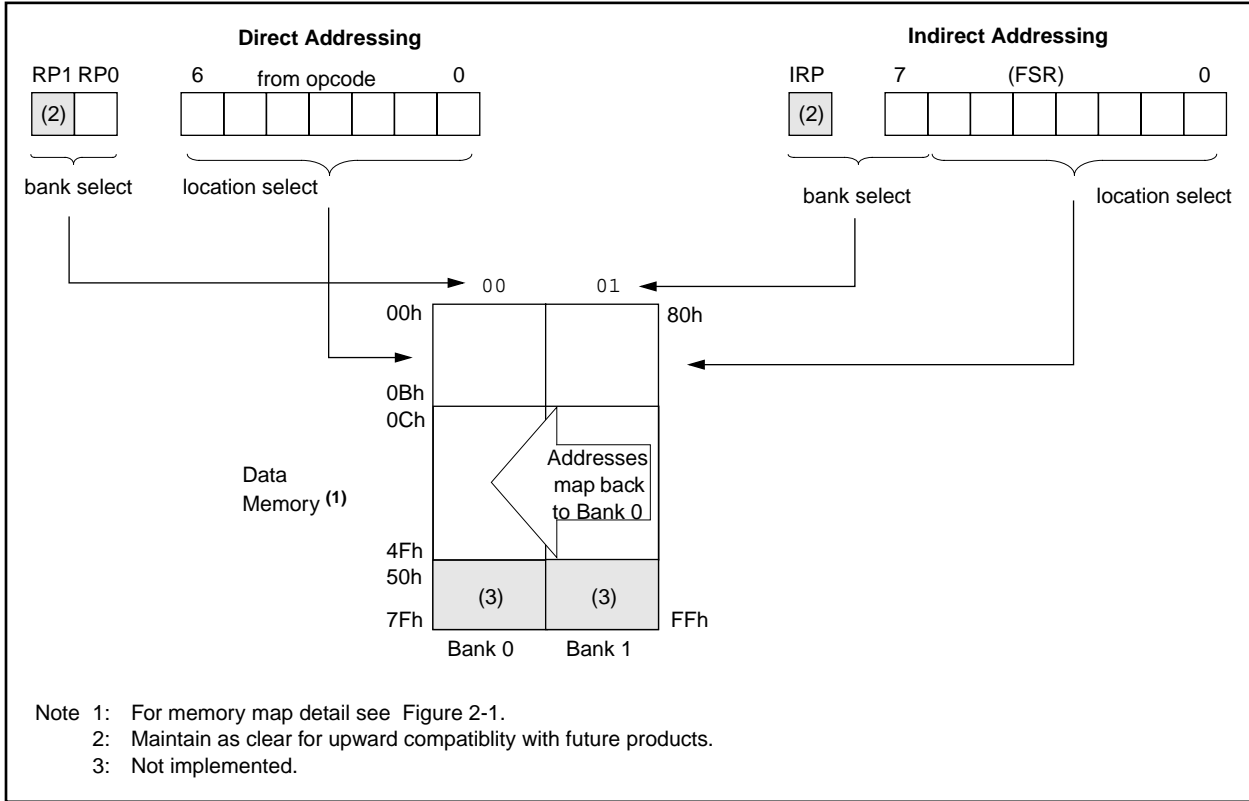
movlw 0x20 ;initialize pointer
movwf FSR ; to RAM
NEXT   clrf INDF ;clear INDF register
       incf FSR ;inc pointer
       btfss FSR,4 ;all done?
       goto NEXT ;NO, clear next

CONTINUE
       : ;YES, continue
    
```

An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 2-1. However, IRP is not used in the PIC16F84A.

PIC16F84A

FIGURE 2-1: DIRECT/INDIRECT ADDRESSING



3.0 I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Additional information on I/O ports may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023).

3.1 PORTA and TRISA Registers

PORTA is a 5-bit wide bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (=1) will make the corresponding PORTA pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output, i.e., put the contents of the output latch on the selected pin.

Note: On a Power-on Reset, these pins are configured as inputs and read as '0'.

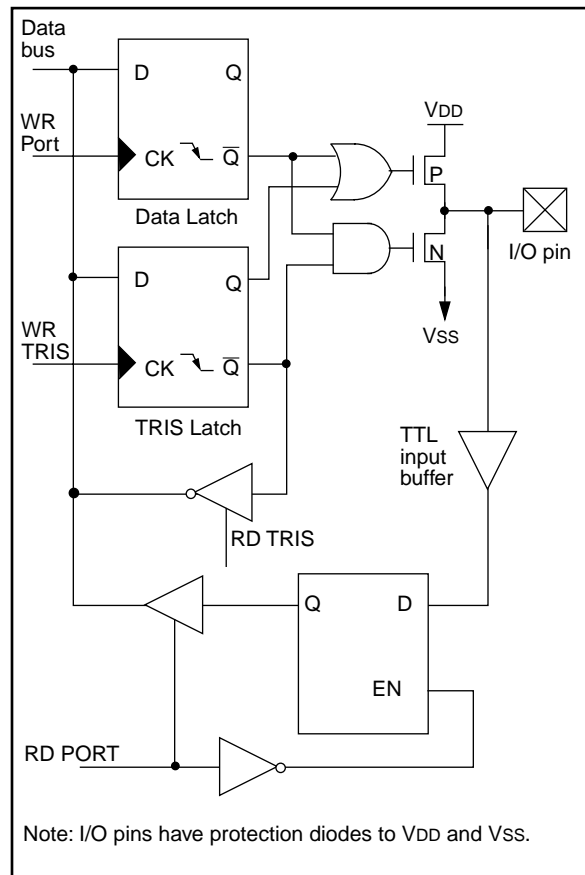
Reading the PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch.

Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers.

EXAMPLE 3-1: INITIALIZING PORTA

```
BCF    STATUS, RP0 ;
CLRF   PORTA      ; Initialize PORTA by
                  ; clearing output
                  ; data latches
BSF    STATUS, RP0 ; Select Bank 1
MOVLW  0x0F      ; Value used to
                  ; initialize data
                  ; direction
MOVWF  TRISA     ; Set RA<3:0> as inputs
                  ; RA4 as output
                  ; TRISA<7:5> are always
                  ; read as '0'.
```

FIGURE 3-1: BLOCK DIAGRAM OF PINS RA3:RA0



PIC16F84A

FIGURE 3-2: BLOCK DIAGRAM OF PIN RA4

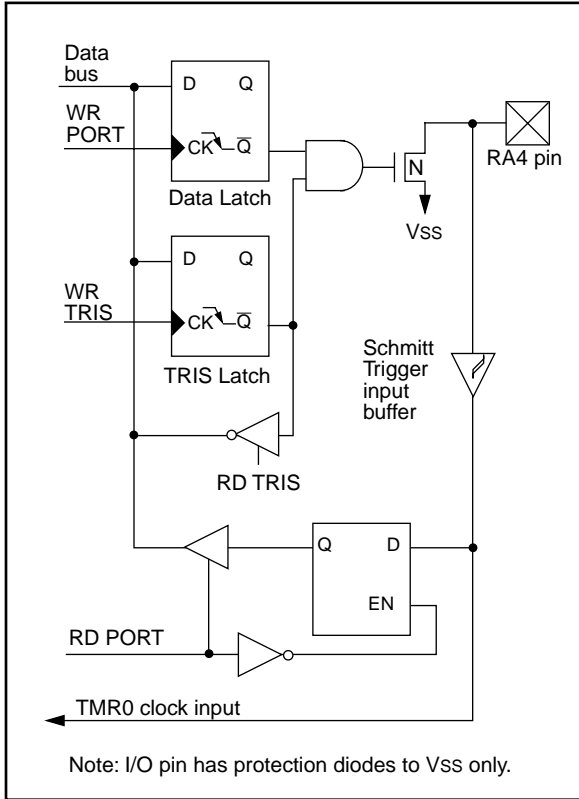


TABLE 3-1 PORTA FUNCTIONS

Name	Bit0	Buffer Type	Function
RA0	bit0	TTL	Input/output
RA1	bit1	TTL	Input/output
RA2	bit2	TTL	Input/output
RA3	bit3	TTL	Input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0. Output is open drain type.

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 3-2 SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
05h	PORTA	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxxx	---u uuuu
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are unimplemented, read as '0'

3.2 PORTB and TRISB Registers

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output, i.e., put the contents of the output latch on the selected pin.

EXAMPLE 3-1: INITIALIZING PORTB

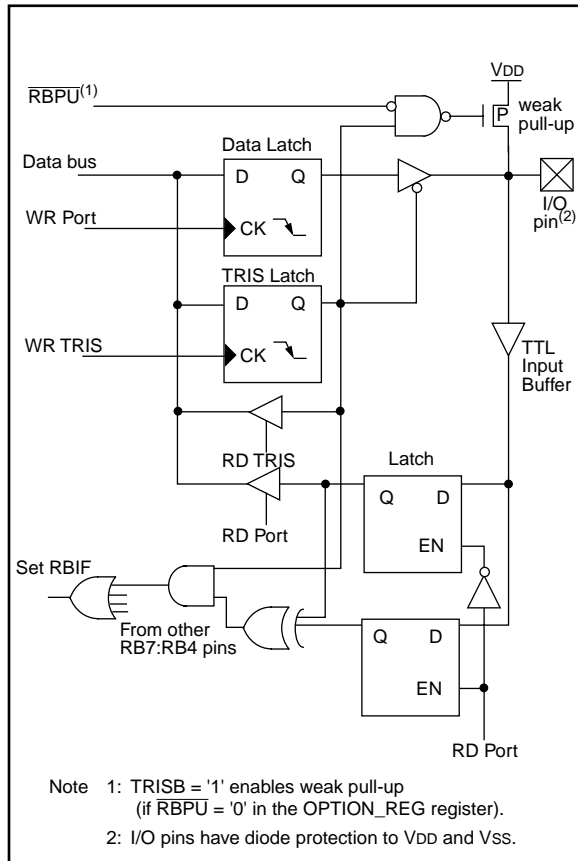
```
BCF STATUS, RP0 ;
CLRF PORTB      ; Initialize PORTB by
                ; clearing output
                ; data latches

BSF STATUS, RP0 ; Select Bank 1
MOVLW 0xCF      ; Value used to
                ; initialize data
                ; direction

MOVWF TRISB     ; Set RB<3:0> as inputs
                ; RB<5:4> as outputs
                ; RB<7:6> as outputs
```

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit $\overline{\text{RBP}}\text{U}$ (OPTION<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

FIGURE 3-3: BLOCK DIAGRAM OF PINS RB7:RB4



Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

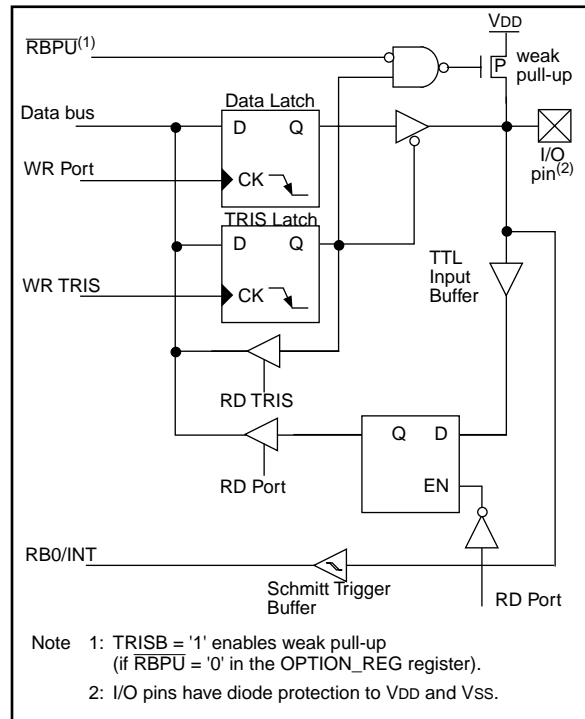
This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

- Any read or write of PORTB. This will end the mismatch condition.
- Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared.

The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

FIGURE 3-4: BLOCK DIAGRAM OF PINS RB3:RB0



PIC16F84A

TABLE 3-3 PORTB FUNCTIONS

Name	Bit	Buffer Type	I/O Consistency Function
RB0/INT	bit0	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST ⁽²⁾	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST ⁽²⁾	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger.

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 3-4 SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	uuuu uuuu
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

4.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- Internal or external clock select
- Edge select for external clock
- 8-bit software programmable prescaler
- Interrupt on overflow from FFh to 00h

Figure 4-1 is a simplified block diagram of the Timer0 module.

Additional information on timer modules is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

4.1 Timer0 Operation

Timer0 can operate as a timer or as a counter.

Timer mode is selected by clearing bit T0CS (OPTION_REG<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS (OPTION_REG<5>). In counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit T0SE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed below.

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (TOSC). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

Additional information on external clock requirements is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

4.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 4-2). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The prescaler is not readable or writable.

The PSA and PS2:PS0 bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

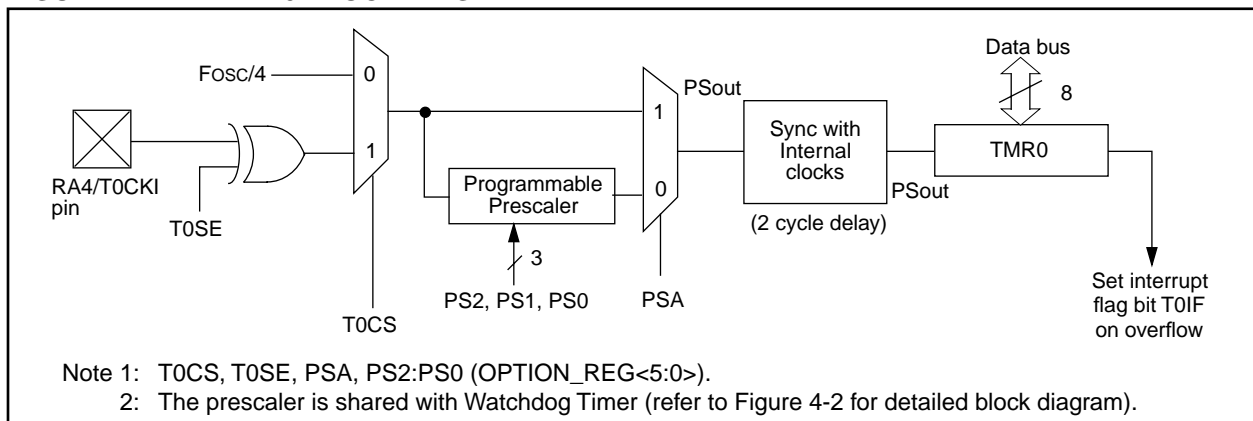
Clearing bit PSA will assign the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable.

Setting bit PSA will assign the prescaler to the Watchdog Timer (WDT). When the prescaler is assigned to the WDT, prescale values of 1:1, 1:2, ..., 1:128 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g. CLRF 1, MOVWF 1, BSF 1,x...etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT.

Note: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

FIGURE 4-1: TIMER0 BLOCK DIAGRAM



PIC16F84A

4.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed “on the fly” during program execution.

Note: To avoid an unintended device RESET, a specific instruction sequence (shown in the PICmicro™ Mid-Range Reference Manual, DS3023) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

4.3 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP since the timer is shut off during SLEEP.

FIGURE 4-2: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

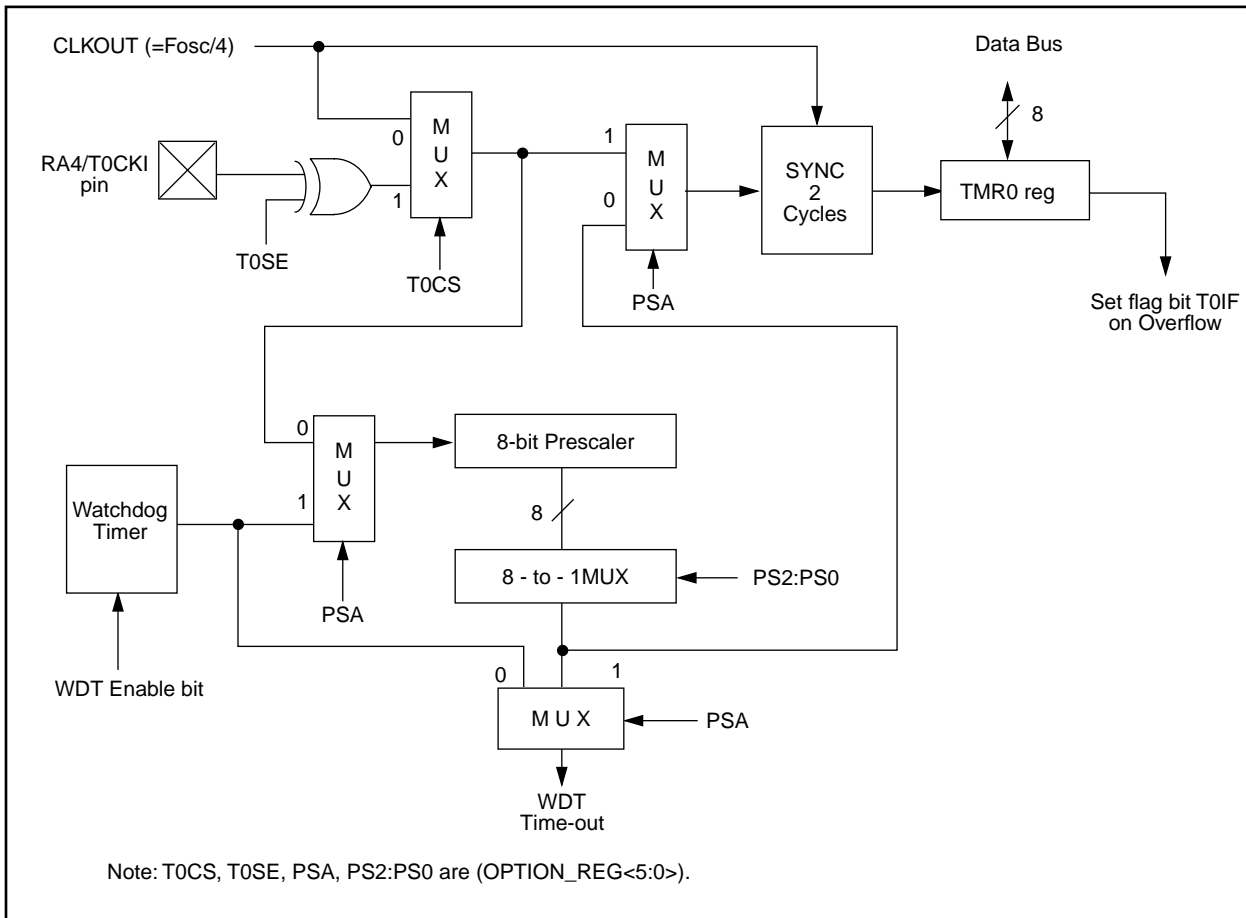


TABLE 4-1 REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
0Bh,8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
81h	OPTION_REG	RBP \bar{U}	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	PORTA Data Direction Register								--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

5.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory. These registers are:

- EECON1
- EECON2 (Not a physically implemented register)
- EEDATA
- EEADR

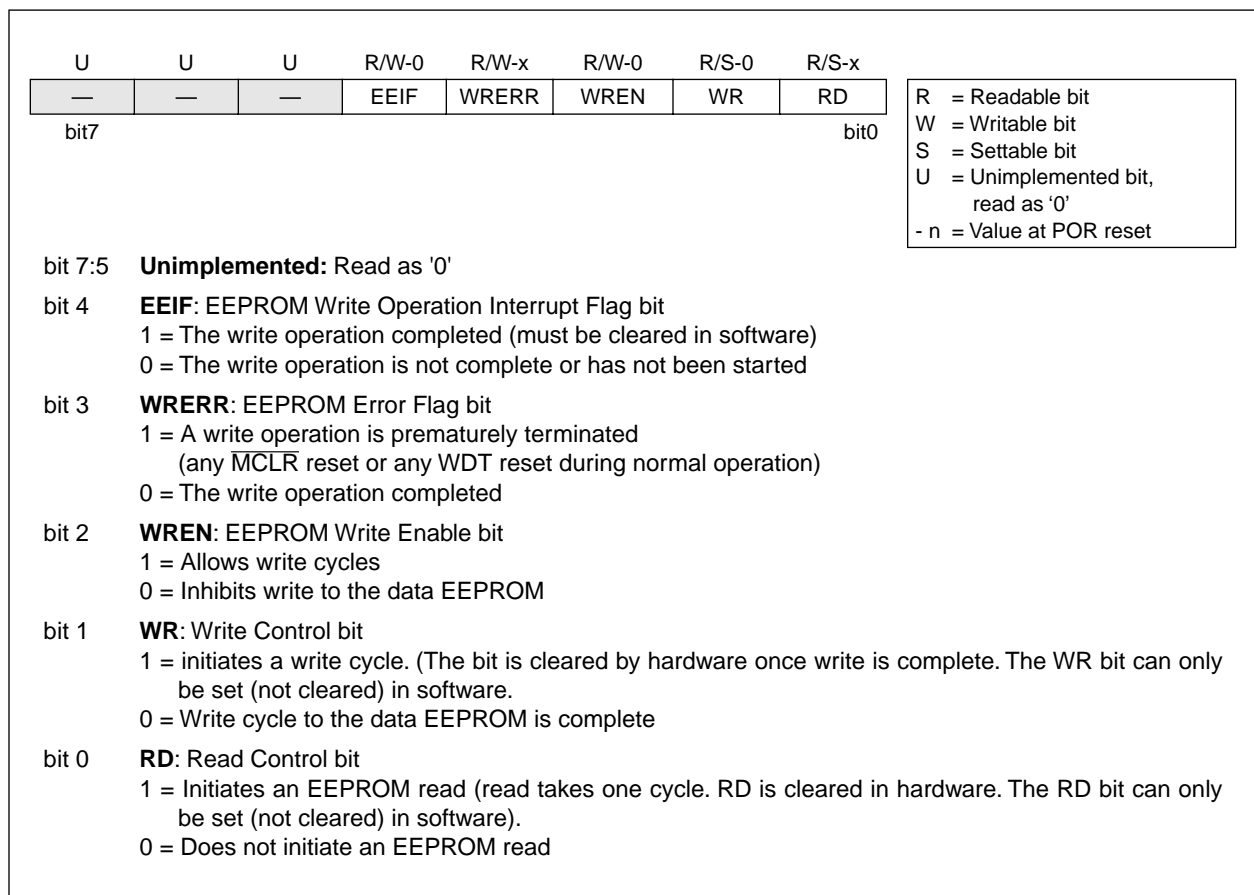
EEDATA holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC16F84A devices have 64 bytes of data EEPROM with an address range from 0h to 3Fh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write-time will vary with voltage and temperature as well as from chip to chip. Please refer to AC specifications for exact limits.

When the device is code protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access this memory.

Additional information on the Data EEPROM is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

FIGURE 5-1: EECON1 REGISTER (ADDRESS 88h)



PIC16F84A

5.1 Reading the EEPROM Data Memory

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD (EECON1<0>). The data is available, in the very next cycle, in the EEDATA register; therefore it can be read in the next instruction. EEDATA will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 5-1: DATA EEPROM READ

```
BCF    STATUS, RP0    ; Bank 0
MOVLW CONFIG_ADDR   ;
MOVWF  EEADR          ; Address to read
BSF    STATUS, RP0    ; Bank 1
BSF    EECON1, RD     ; EE Read
BCF    STATUS, RP0    ; Bank 0
MOVF  EEDATA, W      ; W = EEDATA
```

5.2 Writing to the EEPROM Data Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDATA register. Then the user must follow a specific sequence to initiate the write for each byte.

EXAMPLE 5-1: DATA EEPROM WRITE

```
BSF    STATUS, RP0    ; Bank 1
BCF    INTCON, GIE    ; Disable INTs.
BSF    EECON1, WREN   ; Enable Write
MOVLW  55h            ;
MOVWF  EECON2         ; Write 55h
MOVLW  AAh            ;
MOVWF  EECON2         ; Write AAh
BSF    EECON1, WR     ; Set WR bit
                        ; begin write
BSF    INTCON, GIE    ; Enable INTs.
```

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected)

code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. EEIF must be cleared by software.

5.3 Write Verify

Depending on the application, good programming practice may dictate that the value written to the Data EEPROM should be verified (Example 5-1) to the desired value to be written. This should be used in applications where an EEPROM bit will be stressed near the specification limit. The Total Endurance disk will help determine your comfort level.

Generally the EEPROM write failure will be a bit which was written as a '0', but reads back as a '1' (due to leakage off the bit).

EXAMPLE 5-1: WRITE VERIFY

```
BCF    STATUS, RP0    ; Bank 0
:      ; Any code can go here
:      ;
MOVWF  EEDATA, W      ; Must be in Bank 0
BSF    STATUS, RP0    ; Bank 1
READ
BSF    EECON1, RD     ; YES, Read the
                        ; value written
BCF    STATUS, RP0    ; Bank 0
;
; Is the value written (in W reg) and
; read (in EEDATA) the same?
;
SUBWF  EEDATA, W      ;
BTFS   STATUS, Z       ; Is difference 0?
GOTO   WRITE_ERR     ; NO, Write error
:      ; YES, Good write
:      ; Continue program
```

TABLE 5-1 REGISTERS/BITS ASSOCIATED WITH DATA EEPROM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
08h	EEDATA	EEPROM data register								xxxx xxxx	uuuu uuuu
09h	EEADR	EEPROM address register								xxxx xxxx	uuuu uuuu
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	---0 q000
89h	EECON2	EEPROM control register 2								---- ----	---- ----

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by data EEPROM.

6.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real time applications. The PIC16F84A has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- OSC Selection
- Reset
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-circuit serial programming

The PIC16F84A has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep

the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only. This design keeps the device in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode offers a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer time-out or through an interrupt. Several oscillator options are provided to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select the various options.

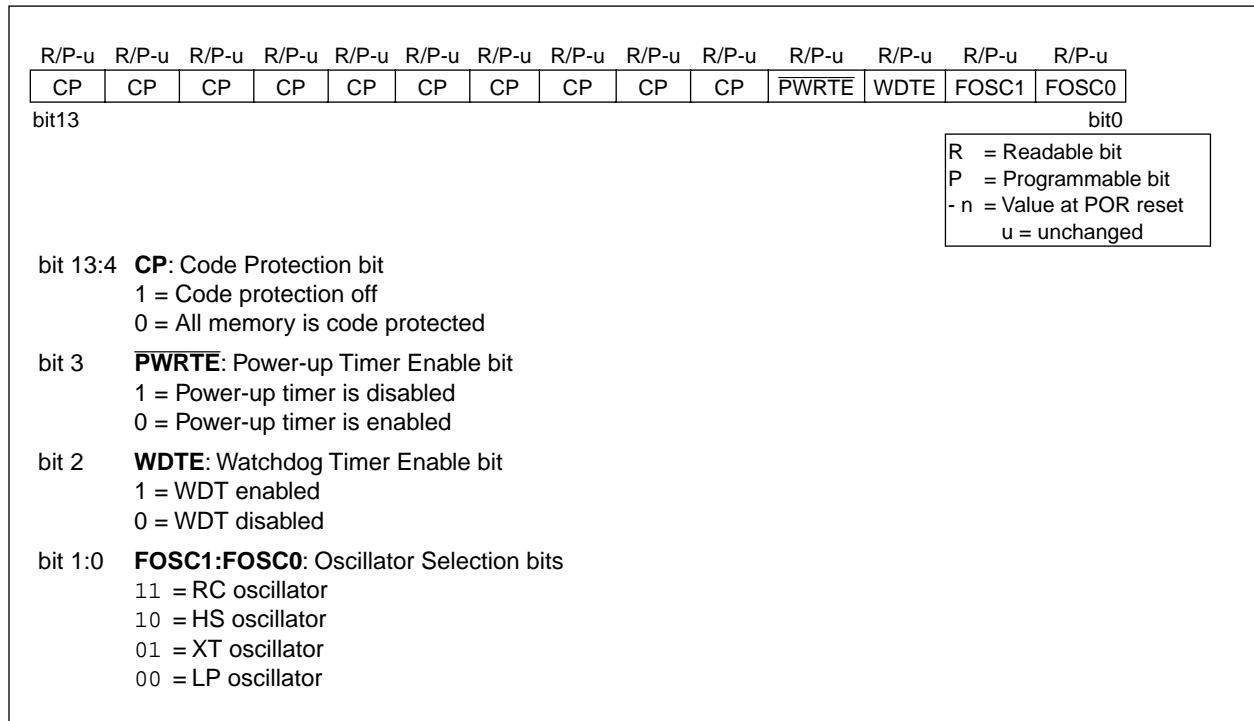
Additional information on special features is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

6.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

Address 2007h is beyond the user program memory space and it belongs to the special test/configuration memory space (2000h - 3FFFh). This space can only be accessed during programming.

FIGURE 6-1: CONFIGURATION WORD - PIC16F84A



PIC16F84A

6.2 Oscillator Configurations

6.2.1 OSCILLATOR TYPES

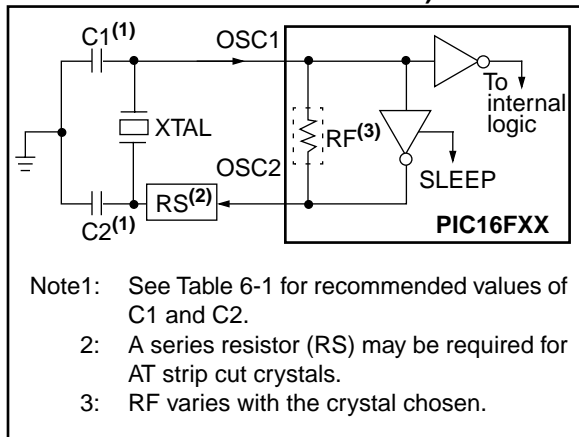
The PIC16F84A can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

6.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 6-2).

FIGURE 6-2: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



The PIC16F84A oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin (Figure 6-3).

FIGURE 6-3: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

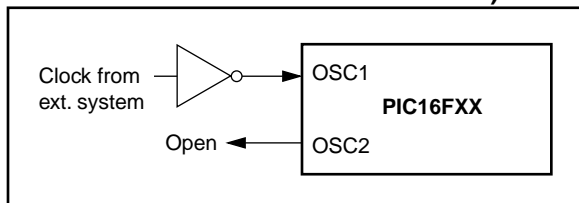


TABLE 6-1 CAPACITOR SELECTION FOR CERAMIC RESONATORS

Ranges Tested:			
Mode	Freq	OSC1/C1	OSC2/C2
XT	455 kHz	47 - 100 pF	47 - 100 pF
	2.0 MHz	15 - 33 pF	15 - 33 pF
	4.0 MHz	15 - 33 pF	15 - 33 pF
HS	8.0 MHz	15 - 33 pF	15 - 33 pF
	10.0 MHz	15 - 33 pF	15 - 33 pF

Note: Recommended values of C1 and C2 are identical to the ranges tested table.
 Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for the appropriate values of external components.

Resonators Tested:

455 kHz	Panasonic EFO-A455K04B	± 0.3%
2.0 MHz	Murata Erie CSA2.00MG	± 0.5%
4.0 MHz	Murata Erie CSA4.00MG	± 0.5%
8.0 MHz	Murata Erie CSA8.00MT	± 0.5%
10.0 MHz	Murata Erie CSA10.00MTZ	± 0.5%

None of the resonators had built-in capacitors.

TABLE 6-2 CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Mode	Freq	OSC1/C1	OSC2/C2
LP	32 kHz	68 - 100 pF	68 - 100 pF
	200 kHz	15 - 33 pF	15 - 33 pF
XT	100 kHz	100 - 150 pF	100 - 150 pF
	2 MHz	15 - 33 pF	15 - 33 pF
	4 MHz	15 - 33 pF	15 - 33 pF
HS	4 MHz	15 - 33 pF	15 - 33 pF
	10 MHz	15 - 33 pF	15 - 33 pF

Note: Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.
 For VDD > 4.5V, C1 = C2 ≈ 30 pF is recommended.

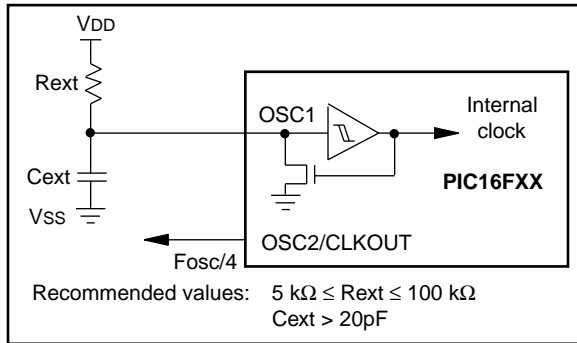
Crystals Tested:

32.768 kHz	Epson C-001R32.768K-A	± 20 PPM
100 kHz	Epson C-2 100.00 KC-P	± 20 PPM
200 kHz	STD XTL 200.000 KHz	± 20 PPM
1.0 MHz	ECS ECS-10-13-2	± 50 PPM
2.0 MHz	ECS ECS-20-S-2	± 50 PPM
4.0 MHz	ECS ECS-40-S-4	± 50 PPM
10.0 MHz	ECS ECS-100-S-4	± 50 PPM

6.2.3 RC OSCILLATOR

For timing insensitive applications the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (R_{ext}) values, capacitor (C_{ext}) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types also affects the oscillation frequency, especially for low C_{ext} values. The user needs to take into account variation due to tolerance of the external R and C components. Figure 6-4 shows how an R/C combination is connected to the PIC16F84A.

FIGURE 6-4: RC OSCILLATOR MODE



6.3 Reset

The PIC16F84A differentiates between various kinds of reset:

- Power-on Reset (POR)
- \overline{MCLR} reset during normal operation
- \overline{MCLR} reset during SLEEP
- WDT Reset (during normal operation)
- WDT Wake-up (during SLEEP)

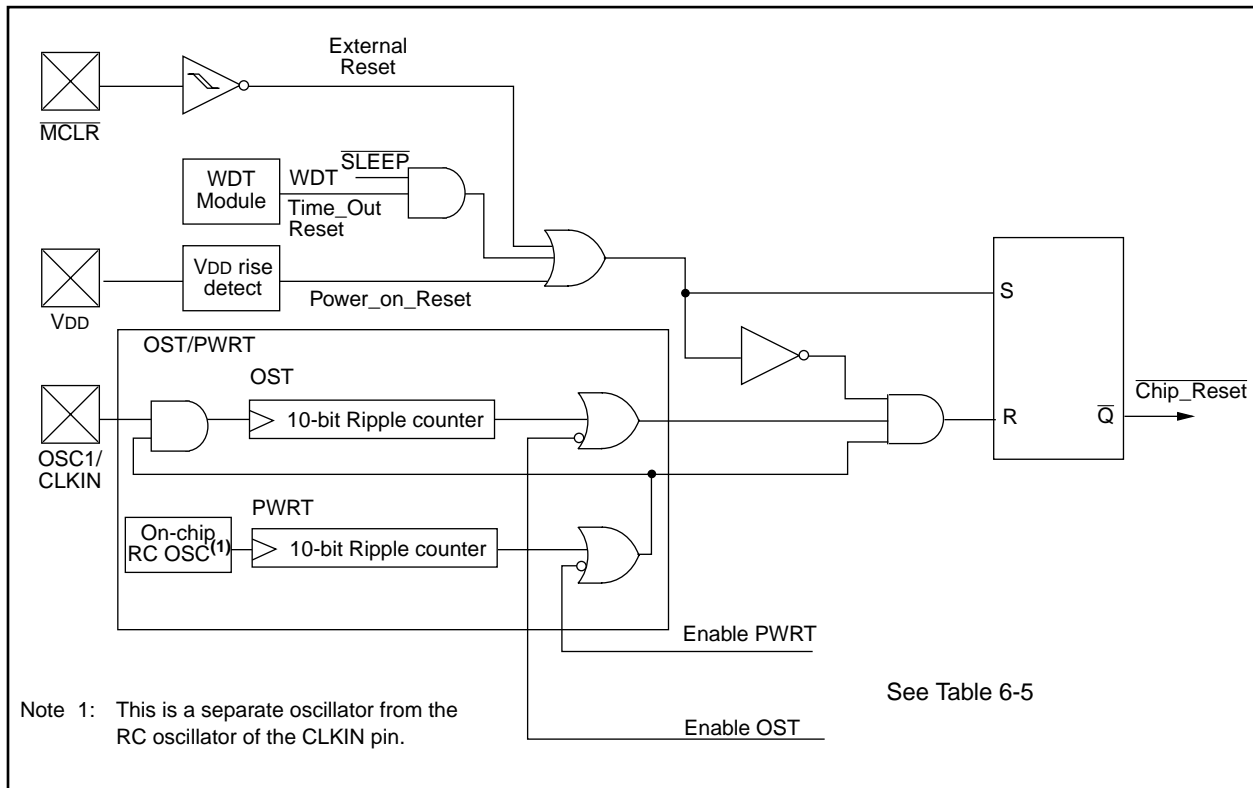
Figure 6-5 shows a simplified block diagram of the on-chip reset circuit. The \overline{MCLR} reset path has a noise filter to ignore small pulses. The electrical specifications state the pulse width requirements for the \overline{MCLR} pin.

Some registers are not affected in any reset condition; their status is unknown on a POR reset and unchanged in any other reset. Most other registers are reset to a "reset state" on POR, \overline{MCLR} or WDT reset during normal operation and on \overline{MCLR} reset during SLEEP. They are not affected by a WDT reset during SLEEP, since this reset is viewed as the resumption of normal operation.

Table 6-3 gives a description of reset conditions for the program counter (PC) and the STATUS register. Table 6-4 gives a full description of reset states for all registers.

The \overline{TO} and \overline{PD} bits are set or cleared differently in different reset situations (Section 6.7). These bits are used in software to determine the nature of the reset.

FIGURE 6-5: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



PIC16F84A

TABLE 6-3 RESET CONDITION FOR PROGRAM COUNTER AND THE STATUS REGISTER

Condition	Program Counter	STATUS Register
Power-on Reset	000h	0001 1xxx
MCLR Reset during normal operation	000h	000u uuuu
MCLR Reset during SLEEP	000h	0001 0uuu
WDT Reset (during normal operation)	000h	0000 1uuu
WDT Wake-up	PC + 1	uuu0 0uuu
Interrupt wake-up from SLEEP	PC + 1 ⁽¹⁾	uuu1 0uuu

Legend: u = unchanged, x = unknown.

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 6-4 RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-on Reset	MCLR Reset during: – normal operation – SLEEP WDT Reset during normal operation	Wake-up from SLEEP: – through interrupt – through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	---- ----	---- ----	---- ----
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000h	0000h	PC + 1 ⁽²⁾
STATUS	03h	0001 1xxx	000q quuu ⁽³⁾	uuuq quuu ⁽³⁾
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA ⁽⁴⁾	05h	---x xxxx	---u uuuu	---u uuuu
PORTB ⁽⁵⁾	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEDATA	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEADR	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu ⁽¹⁾
INDF	80h	---- ----	---- ----	---- ----
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
PCL	82h	0000h	0000h	PC + 1
STATUS	83h	0001 1xxx	000q quuu ⁽³⁾	uuuq quuu ⁽³⁾
FSR	84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TRISA	85h	---1 1111	---1 1111	---u uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
EECON1	88h	---0 x000	---0 q000	---0 uuuu
EECON2	89h	---- ----	---- ----	---- ----
PCLATH	8Ah	---0 0000	---0 0000	---u uuuu
INTCON	8Bh	0000 000x	0000 000u	uuuu uuuu ⁽¹⁾

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0', q = value depends on condition.

Note 1: One or more bits in INTCON will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: Table 6-3 lists the reset value for each specific condition.

4: On any device reset, these pins are configured as inputs.

5: This is the value that will be in the port output latch.

6.4 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.2V - 1.7V). To take advantage of the POR, just tie the $\overline{\text{MCLR}}$ pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A minimum rise time for VDD must be met for this to operate properly. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting."

The POR circuit does not produce an internal reset when VDD declines.

6.5 Power-up Timer (PWRT)

The Power-up Timer (PWRT) provides a fixed 72 ms nominal time-out (TPWRT) from POR (Figure 6-7, Figure 6-8, Figure 6-9 and Figure 6-10). The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level (Possible exception shown in Figure 6-10).

A configuration bit, $\overline{\text{PWRTE}}$, can enable/disable the PWRT. See Figure 6-1 for the operation of the $\overline{\text{PWRTE}}$ bit for a particular device.

The power-up time delay TPWRT will vary from chip to chip due to VDD, temperature, and process variation. See DC parameters for details.

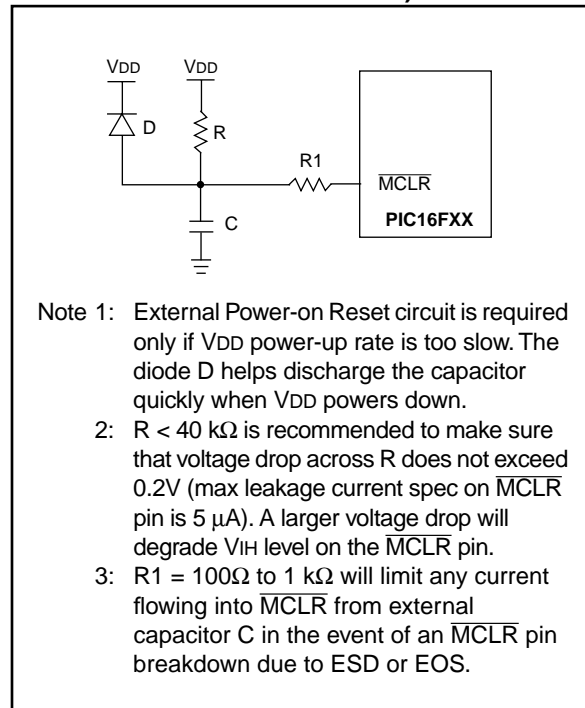
6.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle delay (from OSC1 input) after the PWRT delay ends (Figure 6-7, Figure 6-8, Figure 6-9 and Figure 6-10). This ensures the crystal oscillator or resonator has started and stabilized.

The OST time-out (TOST) is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

When VDD rises very slowly, it is possible that the TPWRT time-out and TOST time-out will expire before VDD has reached its final value. In this case (Figure 6-10), an external power-on reset circuit may be necessary (Figure 6-6).

FIGURE 6-6: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- Note 1: External Power-on Reset circuit is required only if VDD power-up rate is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- 2: $R < 40 \text{ k}\Omega$ is recommended to make sure that voltage drop across R does not exceed 0.2V (max leakage current spec on $\overline{\text{MCLR}}$ pin is $5 \mu\text{A}$). A larger voltage drop will degrade VIH level on the $\overline{\text{MCLR}}$ pin.
- 3: $R1 = 100\Omega$ to $1 \text{ k}\Omega$ will limit any current flowing into MCLR from external capacitor C in the event of an $\overline{\text{MCLR}}$ pin breakdown due to ESD or EOS.

PIC16F84A

FIGURE 6-7: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 1

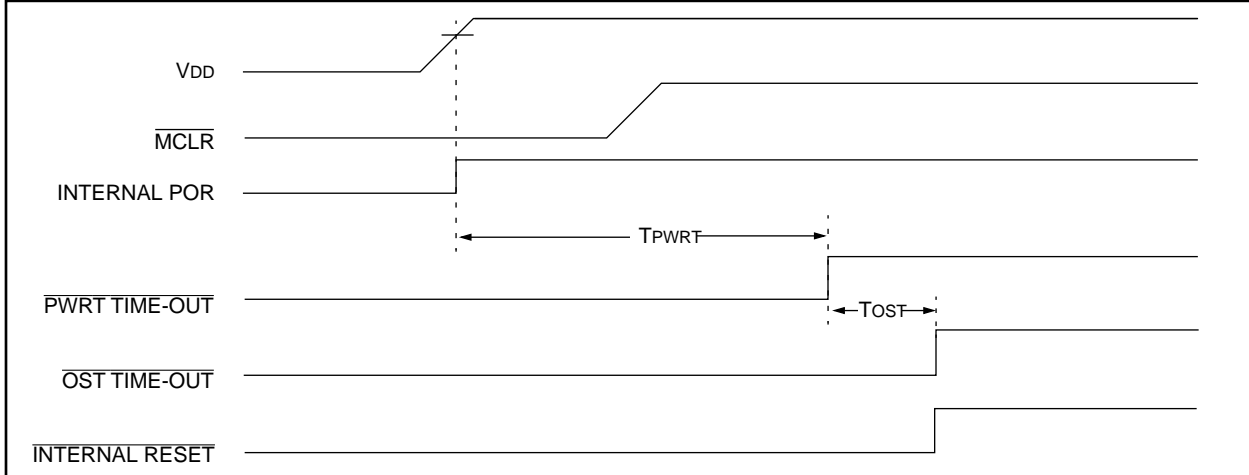


FIGURE 6-8: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 2

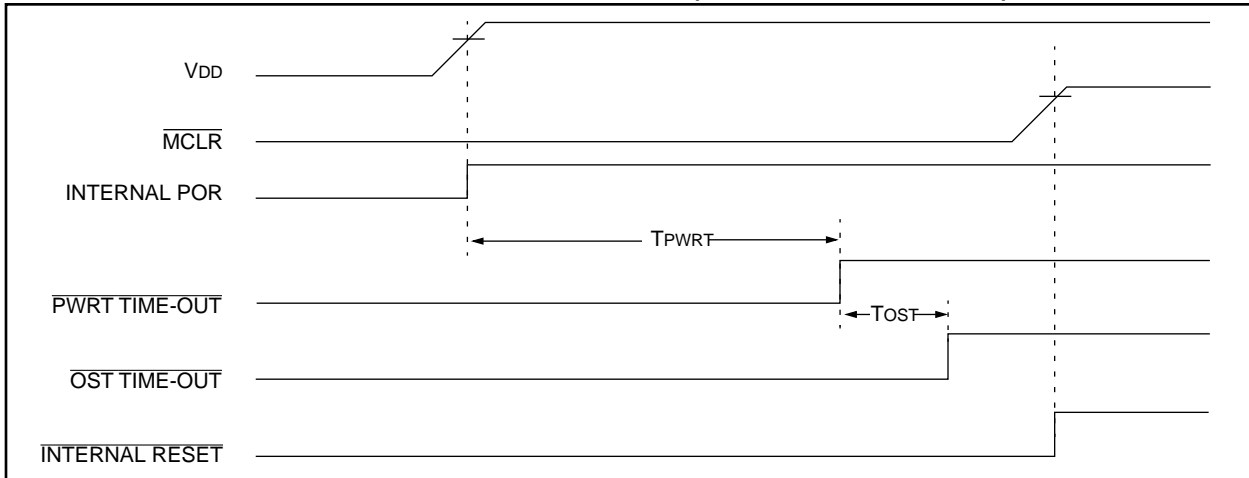


FIGURE 6-9: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD}): FAST V_{DD} RISE TIME

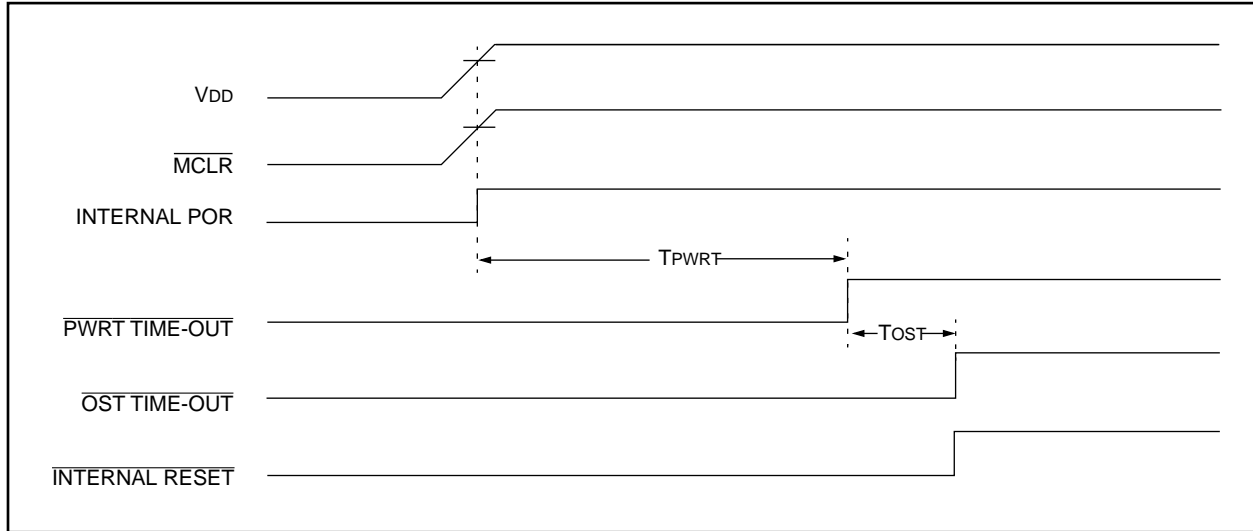
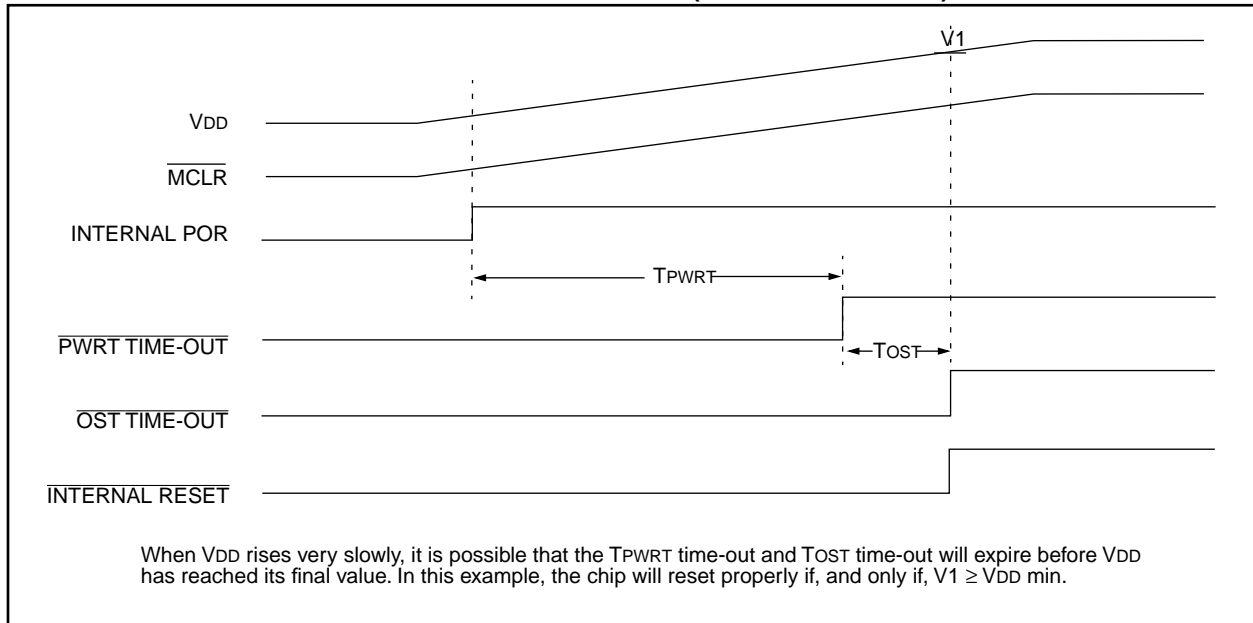


FIGURE 6-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD}): SLOW V_{DD} RISE TIME



PIC16F84A

6.7 Time-out Sequence and Power-down Status Bits (\overline{TO} / \overline{PD})

On power-up (Figure 6-7, Figure 6-8, Figure 6-9 and Figure 6-10) the time-out sequence is as follows: First PWRT time-out is invoked after a POR has expired. Then the OST is activated. The total time-out will vary based on oscillator configuration and PWRTE configuration bit status. For example, in RC mode with the PWRT disabled, there will be no time-out at all.

TABLE 6-5 TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Wake-up from SLEEP
	PWRT Enabled	PWRT Disabled	
XT, HS, LP	72 ms + 1024Tosc	1024Tosc	1024Tosc
RC	72 ms	—	—

Since the time-outs occur from the POR reset pulse, if \overline{MCLR} is kept low long enough, the time-outs will expire. Then bringing \overline{MCLR} high, execution will begin immediately (Figure 6-7). This is useful for testing purposes or to synchronize more than one PIC16F84A device when operating in parallel.

Table 6-6 shows the significance of the \overline{TO} and \overline{PD} bits. Table 6-3 lists the reset conditions for some special registers, while Table 6-4 lists the reset conditions for all the registers.

TABLE 6-6 STATUS BITS AND THEIR SIGNIFICANCE

\overline{TO}	\overline{PD}	Condition
1	1	Power-on Reset
0	x	Illegal, \overline{TO} is set on POR
x	0	Illegal, \overline{PD} is set on POR
0	1	WDT Reset (during normal operation)
0	0	WDT Wake-up
1	1	\overline{MCLR} Reset during normal operation
1	0	\overline{MCLR} Reset during SLEEP or interrupt wake-up from SLEEP

6.8 Interrupts

The PIC16F84A has 4 sources of interrupt:

- External interrupt RB0/INT pin
- TMR0 overflow interrupt
- PORTB change interrupts (pins RB7:RB4)
- Data EEPROM write complete interrupt

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also contains the individual and global interrupt enable bits.

The global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. Bit GIE is cleared on reset.

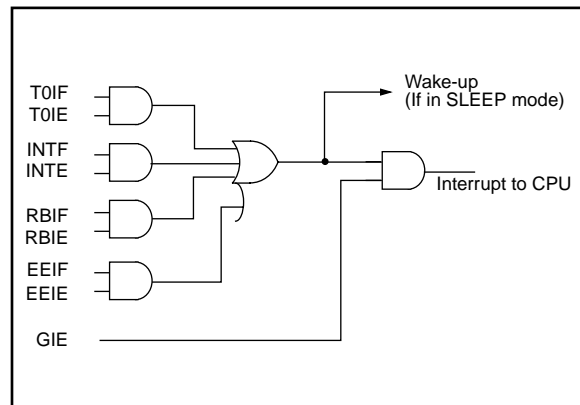
The “return from interrupt” instruction, RETFIE, exits interrupt routine as well as sets the GIE bit, which re-enables interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

When an interrupt is responded to; the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. For external interrupt events, such as the RB0/INT pin or PORTB change interrupt, the interrupt latency will be three to four instruction cycles. The exact latency depends when the interrupt event occurs. The latency is the same for both one and two cycle instructions. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests.

Note 1: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

FIGURE 6-11: INTERRUPT LOGIC



6.8.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if INTEDG bit (OPTION_REG<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing control bit INTE (INTCON<4>). Flag bit INTF must be cleared in software via the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake the processor from SLEEP (Section 6.11) only if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether the processor branches to the interrupt vector following wake-up.

6.8.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in TMR0 will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit TOIE (INTCON<5>) (Section 4.0).

6.8.3 PORB INTERRUPT

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<3>) (Section 3.2).

Note 1: For a change on the I/O pin to be recognized, the pulse width must be at least T_{CY} wide.

6.8.4 DATA EEPROM INTERRUPT

At the completion of a data EEPROM write cycle, flag bit EEIF (EECON1<4>) will be set. The interrupt can be enabled/disabled by setting/clearing enable bit EEIE (INTCON<6>) (Section 5.0).

6.9 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users wish to save key register values during an interrupt (e.g., W register and STATUS register). This is implemented in software.

Example 6-1 stores and restores the STATUS and W register's values. The User defined registers, W_TEMP and STATUS_TEMP are the temporary storage locations for the W and STATUS registers values.

Example 6-1 does the following:

- a) Stores the W register.
- b) Stores the STATUS register in STATUS_TEMP.
- c) Executes the Interrupt Service Routine code.
- d) Restores the STATUS (and bank select bit) register.
- e) Restores the W register.

EXAMPLE 6-1: SAVING STATUS AND W REGISTERS IN RAM

```

PUSH  MOVWF  W_TEMP          ; Copy W to TEMP register,
      SWAPF STATUS, W       ; Swap status to be saved into W
      MOVWF STATUS_TEMP    ; Save status to STATUS_TEMP register
ISR   :
      :                    ;
      :                    ; Interrupt Service Routine
      :                    ; should configure Bank as required
      :                    ;
POP   SWAPF STATUS_TEMP, W  ; Swap nibbles in STATUS_TEMP register
      :                    ; and place result into W
      MOVWF STATUS         ; Move W into STATUS register
      :                    ; (sets bank to original state)
      SWAPF W_TEMP, F      ; Swap nibbles in W_TEMP and place result in W_TEMP
      SWAPF W_TEMP, W      ; Swap nibbles in W_TEMP and place result into W
    
```

PIC16F84A

6.10 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT Wake-up causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming configuration bit WDTE as a '0' (Section 6.1).

6.10.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to

part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION_REG register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler (if assigned to the WDT) and prevent it from timing out and generating a device RESET condition.

The \overline{TO} bit in the STATUS register will be cleared upon a WDT time-out.

6.10.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

FIGURE 6-12: WATCHDOG TIMER BLOCK DIAGRAM

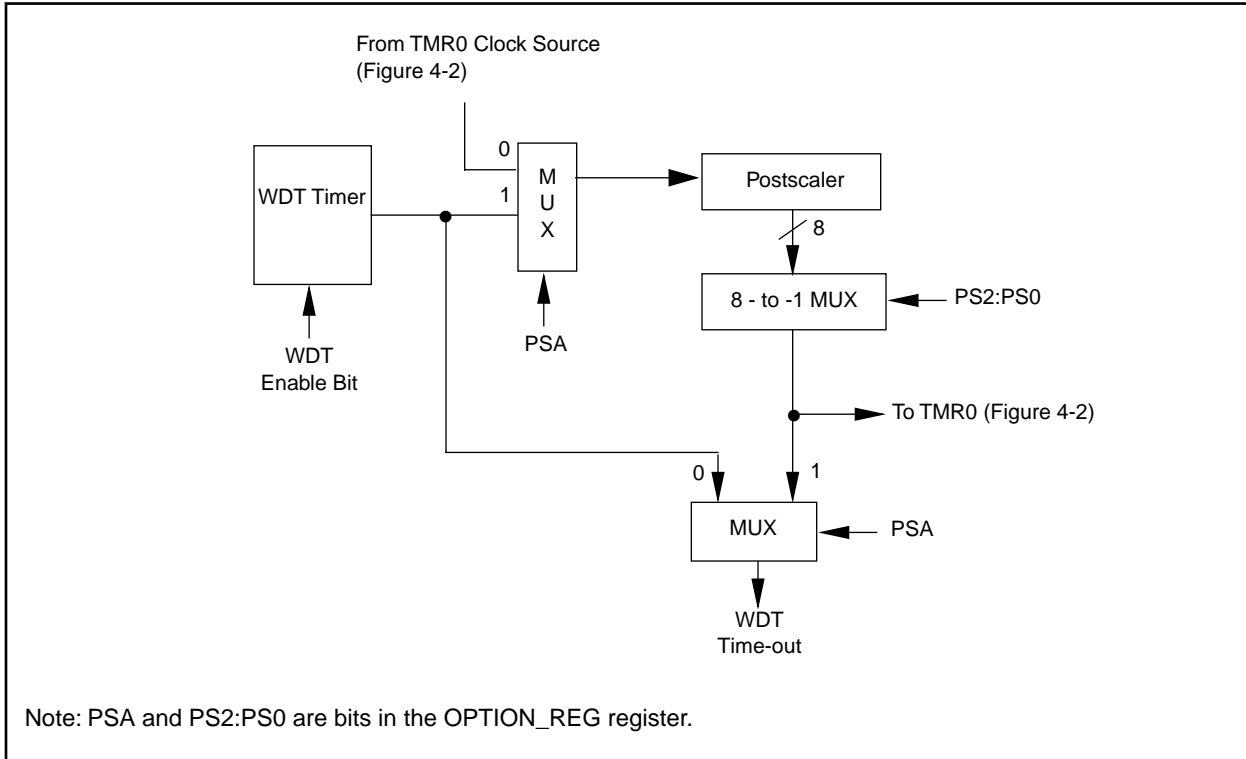


TABLE 6-7 SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
2007h	Config. bits	(2)	(2)	(2)	(2)	PWRTE ⁽¹⁾	WDTE	FOSC1	FOSC0	(2)	
81h	OPTION_REG	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown. Shaded cells are not used by the WDT.

Note 1: See Figure 6-1 for operation of the PWRTE bit.

2: See Figure 6-1 and Section 6.12 for operation of the Code and Data protection bits.

6.11 Power-down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

6.11.1 SLEEP

The Power-down mode is entered by executing the SLEEP instruction.

If enabled, the Watchdog Timer is cleared (but keeps running), the PD bit (STATUS<3>) is cleared, the TO bit (STATUS<4>) is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For the lowest current consumption in SLEEP mode, place all I/O pins at either at VDD or VSS, with no external circuitry drawing current from the I/O pins, and disable external clocks. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or VSS. The contribution from on-chip pull-ups on PORTB should be considered.

The MCLR pin must be at a logic high level (VIHMC).

It should be noted that a RESET generated by a WDT time-out does not drive the MCLR pin low.

6.11.2 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

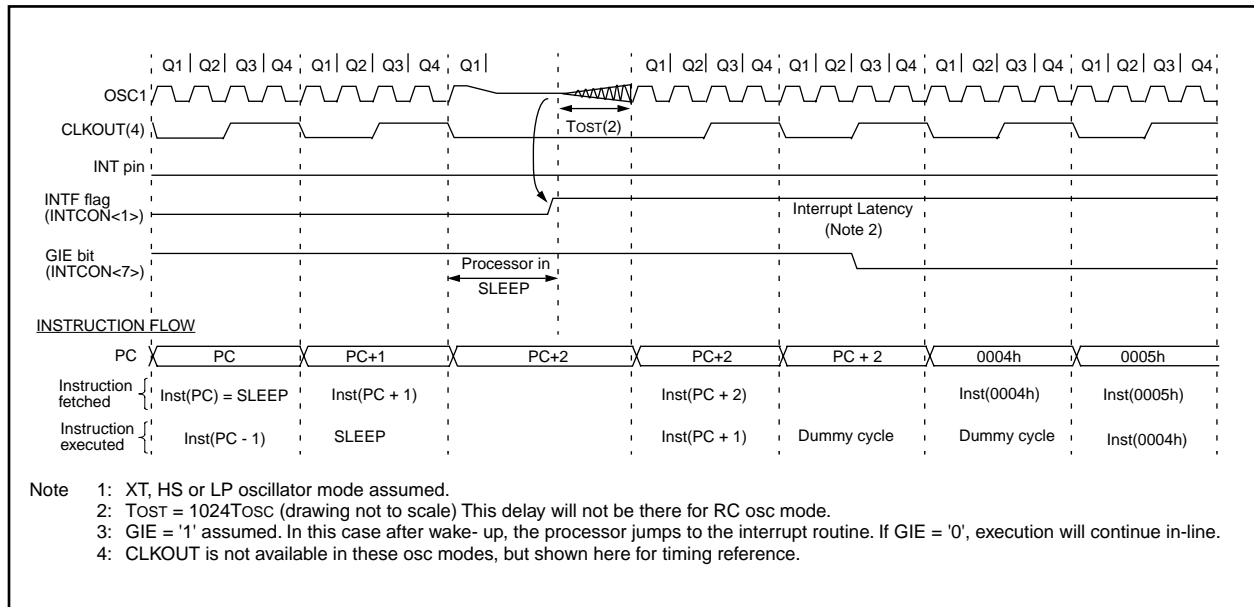
1. External reset input on MCLR pin.
2. WDT Wake-up (if WDT was enabled).
3. Interrupt from RB0/INT pin, RB port change, or data EEPROM write complete.

Peripherals cannot generate interrupts during SLEEP, since no on-chip Q clocks are present.

The first event (MCLR reset) will cause a device reset. The two latter events are considered a continuation of program execution. The TO and PD bits can be used to determine the cause of a device reset. The PD bit, which is set on power-up, is cleared when SLEEP is invoked. The TO bit is cleared if a WDT time-out occurred (and caused wake-up).

While the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

FIGURE 6-13: WAKE-UP FROM SLEEP THROUGH INTERRUPT



6.11.3 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a `SLEEP` instruction, the `SLEEP` instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the \overline{TO} bit will not be set and \overline{PD} bits will not be cleared.
- If the interrupt occurs **during or after** the execution of a `SLEEP` instruction, the device will immediately wake up from sleep. The `SLEEP` instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the \overline{TO} bit will be set and the \overline{PD} bit will be cleared.

Even if the flag bits were checked before executing a `SLEEP` instruction, it may be possible for flag bits to become set before the `SLEEP` instruction completes. To determine whether a `SLEEP` instruction executed, test the \overline{PD} bit. If the \overline{PD} bit is set, the `SLEEP` instruction was executed as a NOP.

To ensure that the WDT is cleared, a `CLRWDT` instruction should be executed before a `SLEEP` instruction.

6.12 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting windowed devices.

6.13 ID Locations

Four memory locations (2000h - 2004h) are designated as ID locations to store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable only during program/verify. Only the four least significant bits of ID location are usable.

6.14 In-Circuit Serial Programming

PIC16F84A microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. Customers can manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product, allowing the most recent firmware or custom firmware to be programmed.

For complete details of serial programming, please refer to the In-Circuit Serial Programming (ICSP™) Guide, (DS30277).

7.0 INSTRUCTION SET SUMMARY

Each PIC16CXXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXX instruction set summary in Table 7-2 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 7-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 7-1 OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
w	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

The instruction set is highly orthogonal and is grouped into three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Table 7-2 lists the instructions recognized by the MPASM assembler.

Figure 7-1 shows the general formats that the instructions can have.

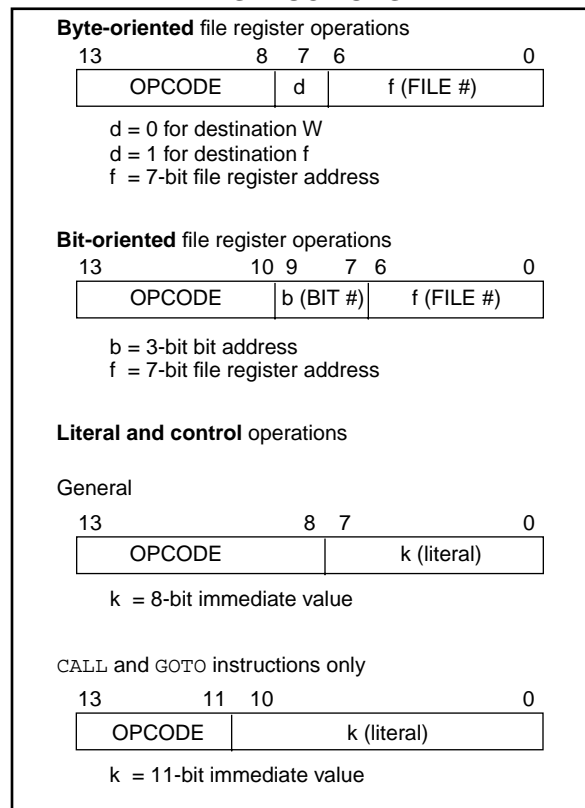
Note: To maintain upward compatibility with future PIC16CXXX products, do not use the **OPTION** and **TRIS** instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 7-1: GENERAL FORMAT FOR INSTRUCTIONS



A description of each instruction is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

PIC16F84A

TABLE 7-2 PIC16CXXX INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	14-Bit Opcode			Status Affected	Notes	
			MSb	LSb				
BYTE-ORIENTED FILE REGISTER OPERATIONS								
ADDWF	f, d	Add W and f	1	00	0111	dfff ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	1fff ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	1fff ffff		
NOP	-	No Operation	1	00	0000	0xx0 0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS								
BCF	f, b	Bit Clear f	1	01	00bb	bfff ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff ffff		3
LITERAL AND CONTROL OPERATIONS								
ADDLW	k	Add literal and W	1	11	111x	kkkk kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110 0100	TO,PD	
GOTO	k	Go to address	2	10	1kkk	kkkk kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000 1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000 1000		
SLEEP	-	Go into standby mode	1	00	0000	0110 0011	TO,PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk kkkk	Z	

- Note 1:** When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- 2:** If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.
- 3:** If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

8.0 DEVELOPMENT SUPPORT

8.1 Development Tools

The PICmicro™ microcontrollers are supported with a full range of hardware and software development tools:

- MPLAB™-ICE Real-Time In-Circuit Emulator
- ICEPIC™ Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE® II Universal Programmer
- PICSTART® Plus Entry-Level Prototype Programmer
- SIMICE
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB™ SIM Software Simulator
- MPLAB-C17 (C Compiler)
- Fuzzy Logic Development System (*fuzzyTECH*®-MP)
- KEELOQ® Evaluation Kits and Programmer

8.2 MPLAB-ICE: High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB-ICE Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers (MCUs). MPLAB-ICE is supplied with the MPLAB Integrated Development Environment (IDE), which allows editing, "make" and download, and source debugging from a single environment.

Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB-ICE allows expansion to support all new Microchip microcontrollers.

The MPLAB-ICE Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows® 3.x or Windows 95 environment were chosen to best make these features available to you, the end user.

MPLAB-ICE is available in two versions. MPLAB-ICE 1000 is a basic, low-cost emulator system with simple trace capabilities. It shares processor modules with the MPLAB-ICE 2000. This is a full-featured emulator system with enhanced trace, trigger, and data monitoring features. Both systems will operate across the entire operating speed range of the PICmicro MCU.

8.3 ICEPIC: Low-Cost PICmicro™ In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC12CXXX, PIC16C5X and PIC16CXXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 386 through Pentium™ based machines under Windows 3.x, Windows 95, or Windows NT environment. ICEPIC features real time, non-intrusive emulation.

8.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode. PRO MATE II is CE compliant.

The PRO MATE II has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode the PRO MATE II can read, verify or program PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices. It can also set configuration and code-protect bits in this mode.

8.5 PICSTART Plus Entry Level Development System

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923, PIC16C924 and PIC17C756 may be supported with an adapter socket. PICSTART Plus is CE compliant.

8.6 SIMICE Entry-Level Hardware Simulator

SIMICE is an entry-level hardware development system designed to operate in a PC-based environment with Microchip's simulator MPLAB™-SIM. Both SIMICE and MPLAB-SIM run under Microchip Technology's MPLAB Integrated Development Environment (IDE) software. Specifically, SIMICE provides hardware simulation for Microchip's PIC12C5XX, PIC12CE5XX, and PIC16C5X families of PICmicro™ 8-bit microcontrollers. SIMICE works in conjunction with MPLAB-SIM to provide non-real-time I/O port emulation. SIMICE enables a developer to run simulator code for driving the target system. In addition, the target system can provide input to the simulator code. This capability allows for simple and interactive debugging without having to manually generate MPLAB-SIM stimulus files. SIMICE is a valuable debugging tool for entry-level system development.

8.7 PICDEM-1 Low-Cost PICmicro Demonstration Board

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-Plus programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the MPLAB-ICE emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

8.8 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I²C bus and separate headers for connection to an LCD module and a keypad.

8.9 PICDEM-3 Low-Cost PIC16CXXX Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

8.10 MPLAB Integrated Development Environment Software

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- A full featured editor
- Three operating modes
 - editor
 - emulator
 - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information
- Extensive on-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PICmicro tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

8.11 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PC-hosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from MPLAB-ICE, Microchip's Universal Emulator System.

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip's emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PICmicro. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

8.12 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PICmicro series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C17 and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

8.13 MPLAB-C17 Compiler

The MPLAB-C17 Code Development System is a complete ANSI 'C' compiler and integrated development environment for Microchip's PIC17CXXX family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display.

8.14 Fuzzy Logic Development System (fuzzyTECH-MP)

fuzzyTECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, *fuzzyTECH-MP*, Edition for implementing more complex systems.

Both versions include Microchip's *fuzzyLAB™* demonstration board for hands-on experience with fuzzy logic systems implementation.

8.15 SEEVAL® Evaluation and Programming System

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

8.16 KEELOQ® Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

	PIC12C5XX	PIC14000	PIC16C5X	PIC16CXXX	PIC16C6X	PIC16C7XX	PIC16C8X	PIC16C9XX	PIC17C4X	PIC17C7XX	24CXX 25CXX 93CXX	HCS200 HCS300 HCS301
Emulator Products												
MPLAB™-ICE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
ICEPIC™ Low-Cost In-Circuit Emulator			✓	✓	✓	✓	✓	✓				
Software Tools												
MPLAB™ Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
MPLAB™ C17* Compiler									✓	✓		
fuzzyTECH®-MP Explorer/Edition Fuzzy Logic Dev. Tool	✓	✓	✓	✓	✓	✓	✓	✓	✓			
Total Endurance™ Software Model											✓	
Programmers												
PICSTART®Plus Low-Cost Universal Dev. Kit	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
PRO MATE® II Universal Programmer	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
KEELOQ® Programmer												✓
Demo Boards												
SEEVAL® Designers Kit											✓	
SIMICE	✓		✓									
PICDEM-14A		✓										
PICDEM-1			✓	✓			✓		✓			
PICDEM-2					✓	✓						
PICDEM-3								✓				
KEELOQ® Evaluation Kit												✓
KEELOQ Transponder Kit												✓

TABLE 8-1: DEVELOPMENT TOOLS FROM MICROCHIP

PIC16F84A

NOTES:

9.0 ELECTRICAL CHARACTERISTICS FOR PIC16F84A

Absolute Maximum Ratings †

Ambient temperature under bias.....	-55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, $\overline{\text{MCLR}}$, and RA4).....	-0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	-0.3 to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to Vss ⁽¹⁾	-0.3 to +14V
Voltage on RA4 with respect to Vss	-0.3 to +8.5V
Total power dissipation ⁽²⁾	800 mW
Maximum current out of Vss pin	150 mA
Maximum current into VDD pin	100 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > VDD).....	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > VDD).....	±20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin	20 mA
Maximum current sunk by PORTA	80 mA
Maximum current sourced by PORTA.....	50 mA
Maximum current sunk by PORTB.....	150 mA
Maximum current sourced by PORTB.....	100 mA

Note 1: Voltage spikes below Vss at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the $\overline{\text{MCLR}}$ pin rather than pulling this pin directly to Vss.

Note 2: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times (I_{DD} + \sum I_{OH}) + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIC16F84A

TABLE 9-1 CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16F84A-04	PIC16F84A-20	PIC16LF84A-04
RC	VDD: 4.0V to 5.5V IDD: 4.5 mA max. at 5.5V IPD: 14 μ A max. at 4V, WDT dis Freq: 4.0 MHz max. at 4V	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 μ A typ. at 5.5V, WDT dis Freq: 4.0 MHz max. at 4V	VDD: 2.0V to 5.5V IDD: 4.5 mA max. at 5.5V IPD: 7.0 μ A max. at 2V WDT dis Freq: 2.0 MHz max. at 2V
XT	VDD: 4.0V to 5.5V IDD: 4.5 mA max. at 5.5V IPD: 14 μ A max. at 4V, WDT dis Freq: 4.0 MHz max. at 4V	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 μ A typ. at 5.5V, WDT dis Freq: 4.0 MHz max. at 4.5V	VDD: 2.0V to 5.5V IDD: 4.5 mA max. at 5.5V IPD: 7.0 μ A max. at 2V WDT dis Freq: 2.0 MHz max. at 2V
HS	VDD: 4.5V to 5.5V IDD: 4.5 mA typ. at 5.5V IPD: 1.0 μ A typ. at 4.5V, WDT dis Freq: 4.0 MHz max. at 4.5V	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V typ. IPD: 1.0 μ A typ. at 4.5V, WDT dis Freq: 20 MHz max. at 4.5V	Do not use in HS mode
LP	VDD: 4.0V to 5.5V IDD: 48 μ A typ. at 32 kHz, 2.0V IPD: 0.6 μ A typ. at 3.0V, WDT dis Freq: 200 kHz max. at 4V	Do not use in LP mode	VDD: 2.0V to 5.5V IDD: 45 μ A max. at 32 kHz, 2.0V IPD: 7 μ A max. at 2.0V WDT dis Freq: 200 kHz max. at 2V

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

PRELIMINARY

9.1 DC CHARACTERISTICS: PIC16F84A-04 (Commercial, Industrial) PIC16F84A-20 (Commercial, Industrial)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial)				
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001 D001A	VDD	Supply Voltage	4.0 4.5	—	5.5 5.5	V V	XT, RC and LP osc configuration HS osc configuration
D002*	VDR	RAM Data Retention Voltage (Note 1)	1.5*	—	—	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004* D004A*	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05* TBD	— —	— —	V/ms	PWRT enabled (PWRTSE bit clear) PWRT disabled (PWRTSE bit set) See section on Power-on Reset for details
D010 D010A	IDD	Supply Current (Note 2)	— —	1.8 3	4.5 10	mA mA	RC and XT osc configuration (Note 4) $F_{\text{OSC}} = 4.0 \text{ MHz}$, $V_{\text{DD}} = 5.5\text{V}$ $F_{\text{OSC}} = 4.0 \text{ MHz}$, $V_{\text{DD}} = 5.5\text{V}$ (During Flash programming)
D013			—	10	20	mA	HS osc configuration (PIC16F84A-20) $F_{\text{OSC}} = 20 \text{ MHz}$, $V_{\text{DD}} = 5.5\text{V}$
D020 D021 D021A	IPD	Power-down Current (Note 3)	— — —	7.0 1.0 1.0	28 14 16	μA μA μA	$V_{\text{DD}} = 4.0\text{V}$, WDT enabled, industrial $V_{\text{DD}} = 4.0\text{V}$, WDT disabled, commercial $V_{\text{DD}} = 4.0\text{V}$, WDT disabled, industrial
D022*	$\Delta\text{I}_{\text{WDT}}$	Module Differential Current (Note 5) Watchdog Timer	— —	6.0 —	20* 25*	μA μA	WDTSE bit set, $V_{\text{DD}} = 4.0\text{V}$, commercial WDTSE bit set, $V_{\text{DD}} = 4.0\text{V}$, extended

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which V_{DD} can be lowered without losing RAM data.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all I_{DD} measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to V_{DD} , T0CKI = V_{DD} , MCLR = V_{DD} ; WDT enabled/disabled as specified.

Note 3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} and V_{SS} .

Note 4: For RC osc configuration, current through R_{ext} is not included. The current through the resistor can be estimated by the formula $I_{\text{R}} = V_{\text{DD}}/2R_{\text{ext}}$ (mA) with R_{ext} in kOhm.

Note 5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base I_{DD} measurement.

PIC16F84A

9.2 DC CHARACTERISTICS: PIC16LF84A-04 (Commercial, Industrial)

DC Characteristics		Standard Operating Conditions (unless otherwise stated)					
Power Supply Pins		Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)					
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	2.0	—	5.5	V	XT, RC, and LP osc configuration
D002*	VDR	RAM Data Retention Voltage (Note 1)	1.5*	—	—	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004* D004A*	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05* TBD	— —	— —	V/ms	PWRT enabled (PWRT _{EN} bit clear) PWRT disabled (PWRT _{EN} bit set) See section on Power-on Reset for details
D010 D010A D014	IDD	Supply Current (Note 2)	— — —	1 3 15	4 10 45	mA mA μA	RC and XT osc configuration (Note 4) Fosc = 2.0 MHz, VDD = 5.5V Fosc = 2.0 MHz, VDD = 5.5V (During Flash programming) LP osc configuration Fosc = 32 kHz, VDD = 2.0V, WDT disabled
D020 D021 D021A	IPD	Power-down Current (Note 3)	— — —	3.0 0.4 0.4	16 7.0 9.0	μA μA μA	VDD = 2.0V, WDT enabled, industrial VDD = 2.0V, WDT disabled, commercial VDD = 2.0V, WDT disabled, industrial
D022*	ΔIWDT	Module Differential Current (Note 5) Watchdog Timer	— —	6.0 —	20* 25*	μA μA	WDTE bit set, VDD = 4.0V, commercial WDTE bit set, VDD = 4.0V, industrial

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_R = V_{DD}/2R_{ext}$ (mA) with Rext in kOhm.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD measurement.

**9.3 DC CHARACTERISTICS: PIC16F84A-04 (Commercial, Industrial)
PIC16F84A-20 (Commercial, Industrial)
PIC16LF84A-04 (Commercial, Industrial)**

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise stated) Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) Operating voltage V_{DD} range as described in DC spec Section 9.1 and Section 9.2.					
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D030 D030A D031 D032 D033 D034	V_{IL}	Input Low Voltage I/O ports with TTL buffer with Schmitt Trigger buffer MCLR, RA4/T0CKI OSC1 (XT, HS and LP modes) OSC1 (RC mode)	V_{SS} V_{SS} V_{SS} V_{SS} V_{SS} V_{SS}	— — — — — —	0.8 0.16 V_{DD} 0.2 V_{DD} 0.2 V_{DD} 0.3 V_{DD} 0.1 V_{DD}	V V V V V V	$4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$ (Note 4) entire range (Note 4) entire range (Note 1)
D040 D040A D041 D042 D043 D043A	V_{IH}	Input High Voltage I/O ports with TTL buffer with Schmitt Trigger buffer MCLR, RA4/T0CKI OSC1 (XT, HS and LP modes) OSC1 (RC mode)	2.0 0.25 V_{DD} +0.8 0.8 V_{DD} 0.8 V_{DD} 0.7 V_{DD} 0.9 V_{DD}	— — — — — — —	V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD}	V V V V V V V	$4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$ (Note 4) entire range (Note 4) entire range (Note 1)
D050	V_{HYS}	Hysteresis of Schmitt Trigger inputs	—	0.1	—	V	
D070	IPURB	PORTB weak pull-up current	50*	250*	400*	μA	$V_{DD} = 5.0\text{V}$, $V_{PIN} = V_{SS}$
D060 D061 D063	I_{IL}	Input Leakage Current (Note 2,3) I/O ports MCLR, RA4/T0CKI OSC1	— — —	— — —	± 1 ± 5 ± 5	μA μA μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at hi-impedance $V_{SS} \leq V_{PIN} \leq V_{DD}$ $V_{SS} \leq V_{PIN} \leq V_{DD}$, XT, HS and LP osc configuration

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. Do not drive the PIC16F84A with an external clock while the device is in RC mode, or chip damage may result.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: The user may choose the better of the two specs.

PIC16F84A

9.4 DC CHARACTERISTICS: PIC16F84A-04 (Commercial, Industrial) PIC16F84A-20 (Commercial, Industrial) PIC16LF84A-04 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise stated) Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) Operating voltage V_{DD} range as described in DC spec Section 9.1 and Section 9.2.					
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D080 D083	VOL	Output Low Voltage I/O ports OSC2/CLKOUT	—	—	0.6	V	$I_{OL} = 8.5\text{ mA}$, $V_{DD} = 4.5\text{V}$ $I_{OL} = 1.6\text{ mA}$, $V_{DD} = 4.5\text{V}$, (RC Mode Only)
D090 D092	VOH	Output High Voltage I/O ports (Note 3) OSC2/CLKOUT (Note 3)	$V_{DD}-0.7$ $V_{DD}-0.7$	—	—	V	$I_{OH} = -3.0\text{ mA}$, $V_{DD} = 4.5\text{V}$ $I_{OH} = -1.3\text{ mA}$, $V_{DD} = 4.5\text{V}$ (RC Mode Only)
D150	VOD	Open Drain High Voltage RA4 pin	—	—	8.5	V	
D100	Cosc2	Capacitive Loading Specs on Output Pins OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (RC mode)	—	—	50	pF	
D120 D121	Ed VDRW	Data EEPROM Memory Endurance VDD for read/write	1M* V _{MIN}	10M	—	E/W V	25°C at 5V V _{MIN} = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	4	8*	ms	
D130 D131	EP VPR	Program Flash Memory Endurance VDD for read	100* V _{MIN}	1000	—	E/W V	
D132 D133	VPEW TPEW	VDD for erase/write Erase/Write cycle time	4.5 —	—	5.5	V ms	V _{MIN} = Minimum operating voltage

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. Do not drive the PIC16F84A with an external clock while the device is in RC mode, or chip damage may result.
- 2:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as coming out of the pin.
- 4:** The user may choose the better of the two specs.

9.5 AC (Timing) Characteristics

9.5.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase symbols (pp) and their meanings:

pp			
2	to	os,osc	OSC1
ck	CLKOUT	ost	oscillator start-up timer
cy	cycle time	pwrt	power-up timer
io	I/O port	rbt	RBx pins
inp	INT pin	t0	T0CKI
mc	MCLR	wdt	watchdog timer

Uppercase symbols and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	High Impedance

PRELIMINARY

PIC16F84A

9.5.2 TIMING CONDITIONS

The temperature and voltages specified in Table 9-2 apply to all timing specifications unless otherwise noted. All timings are measure between high and low measurement points as indicated in Figure 9-1. Figure 9-2 specifies the load conditions for the timing specifications.

TABLE 9-2 TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC

Standard Operating Conditions (unless otherwise stated)	
AC CHARACTERISTICS	Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial
	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial
	Operating voltage V_{DD} range as described in DC spec Section 9.1 and Section 9.2

FIGURE 9-1: PARAMETER MEASUREMENT INFORMATION

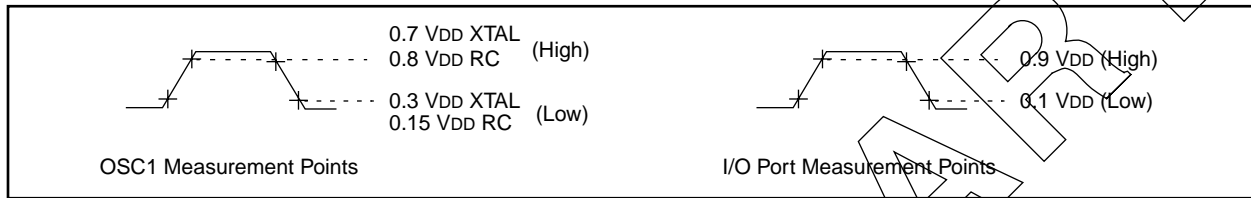
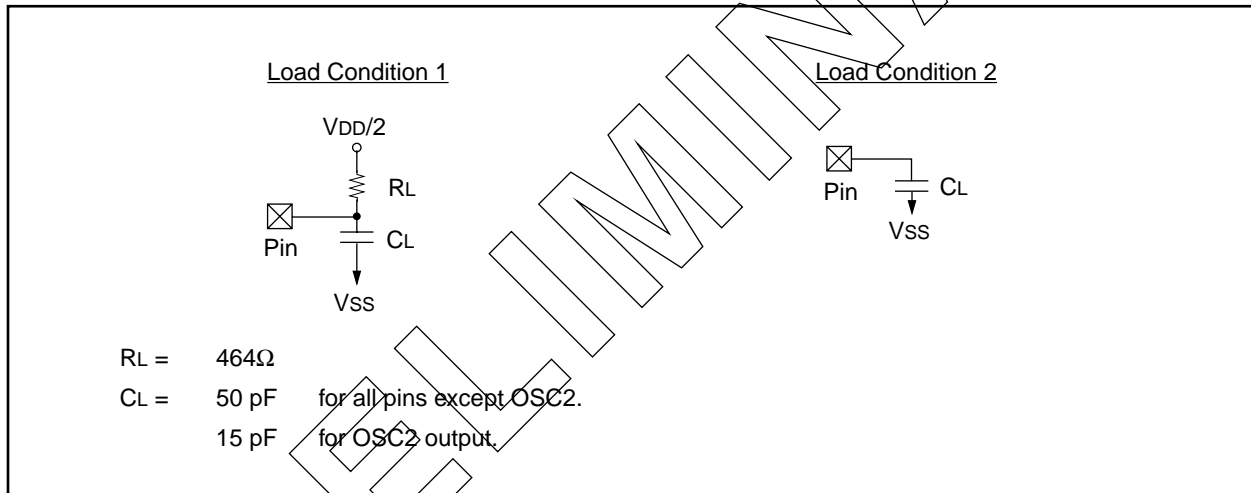


FIGURE 9-2: LOAD CONDITIONS



9.5.3 TIMING DIAGRAMS AND SPECIFICATIONS

FIGURE 9-3: EXTERNAL CLOCK TIMING

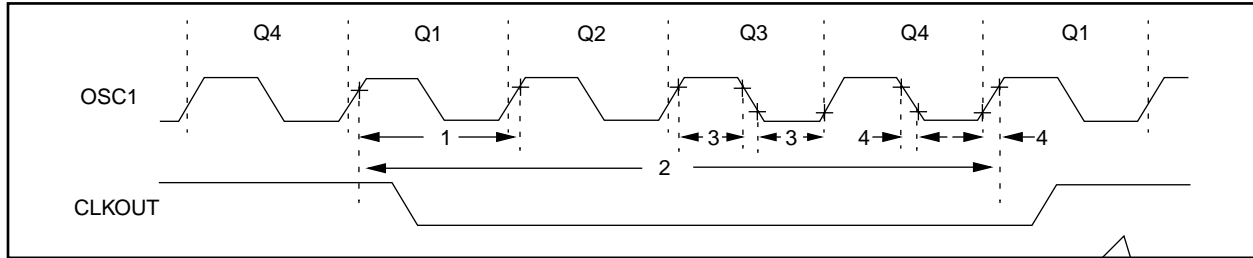


TABLE 9-3 EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions			
	Fosc	External CLKIN Frequency ⁽¹⁾	DC	—	2	MHz	XT, RC osc (-04, LF)			
			DC	—	4	MHz	XT, RC osc (-04)			
			DC	—	20	MHz	HS osc (-20)			
			DC	—	200	kHz	LP osc (-04, LF)			
			Oscillator Frequency ⁽¹⁾	DC	—	2	MHz	RC osc (-04, LF)		
				DC	—	4	MHz	RC osc (-04)		
				0.1	—	2	MHz	XT osc (-04, LF)		
				0.1	—	4	MHz	XT osc (-04)		
			1.0	—	20	MHz	HS osc (-20)			
			DC	—	200	kHz	LP osc (-04, LF)			
			1	Tosc	External CLKIN Period ⁽¹⁾	500	—	—	ns	XT, RC osc (-04, LF)
			250			—	—	ns	XT, RC osc (-04)	
100	—	—	ns			HS osc (-20)				
5.0	—	—	μs			LP osc (-04, LF)				
		Oscillator Period ⁽¹⁾	500	—	—	ns	RC osc (-04, LF)			
			250	—	—	ns	RC osc (-04)			
			500	—	10,000	ns	XT osc (-04, LF)			
			250	—	10,000	ns	XT osc (-04)			
			100	—	1,000	ns	HS osc (-20)			
			5.0	—	—	μs	LP osc (-04, LF)			
2	Tcy	Instruction Cycle Time ⁽¹⁾	0.4	4/Fosc	DC	μs				
3	TosL, TosH	Clock in (OSC1) High or Low Time	60 *	—	—	ns	XT osc (-04, LF)			
			50 *	—	—	ns	XT osc (-04)			
			2.0 *	—	—	μs	LP osc (-04, LF)			
			35 *	—	—	ns	HS osc (-20)			
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	25 *	—	—	ns	XT osc (-04)			
			50 *	—	—	ns	LP osc (-04, LF)			
			15 *	—	—	ns	HS osc (-20)			

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

PIC16F84A

FIGURE 9-4: CLKOUT AND I/O TIMING

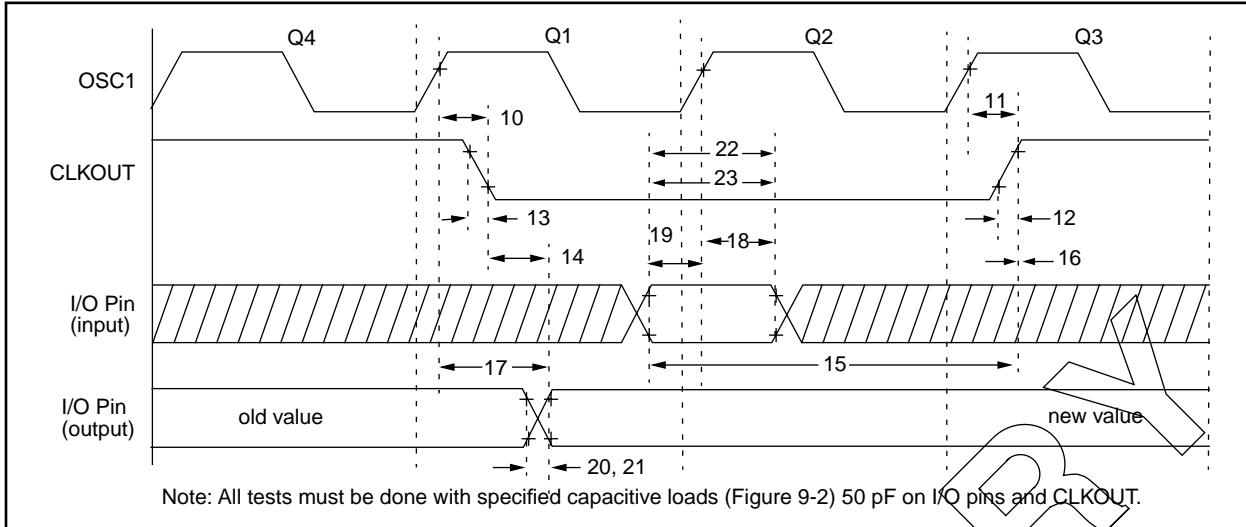


TABLE 9-4 CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓	Standard	15	30 *	ns	Note 1
10A			Extended (LF)	15	120 *	ns	Note 1
11	TosH2ckH	OSC1↑ to CLKOUT↑	Standard	15	30 *	ns	Note 1
11A			Extended (LF)	15	120 *	ns	Note 1
12	TckR	CLKOUT rise time	Standard	15	30 *	ns	Note 1
12A			Extended (LF)	15	100 *	ns	Note 1
13	TckF	CLKOUT fall time	Standard	15	30 *	ns	Note 1
13A			Extended (LF)	15	100 *	ns	Note 1
14	TckL2ioV	CLKOUT ↓ to Port out valid	—	—	0.5Tcy + 20 *	ns	Note 1
15	TioV2ckH	Port in valid before CLKOUT ↑	Standard	0.30Tcy + 30 *	—	ns	Note 1
			Extended (LF)	0.30Tcy + 80 *	—	ns	Note 1
16	TckH2ioI	Port in hold after CLKOUT ↑	0 *	—	—	ns	Note 1
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	Standard	—	125 *	ns	
			Extended (LF)	—	250 *	ns	
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	Standard	10 *	—	ns	
			Extended (LF)	10 *	—	ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	Standard	-75 *	—	ns	
			Extended (LF)	-175 *	—	ns	
20	TioR	Port output rise time	Standard	10	35 *	ns	
20A			Extended (LF)	10	70 *	ns	
21	TioF	Port output fall time	Standard	10	35 *	ns	
21A			Extended (LF)	10	70 *	ns	
22	Tinp	INT pin high or low time	Standard	20 *	—	ns	
22A			Extended (LF)	55 *	—	ns	
23	Trbp	RB7:RB4 change INT high or low time	Standard	Tosc §	—	ns	
23A			Extended (LF)	Tosc §	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ By design

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

FIGURE 9-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

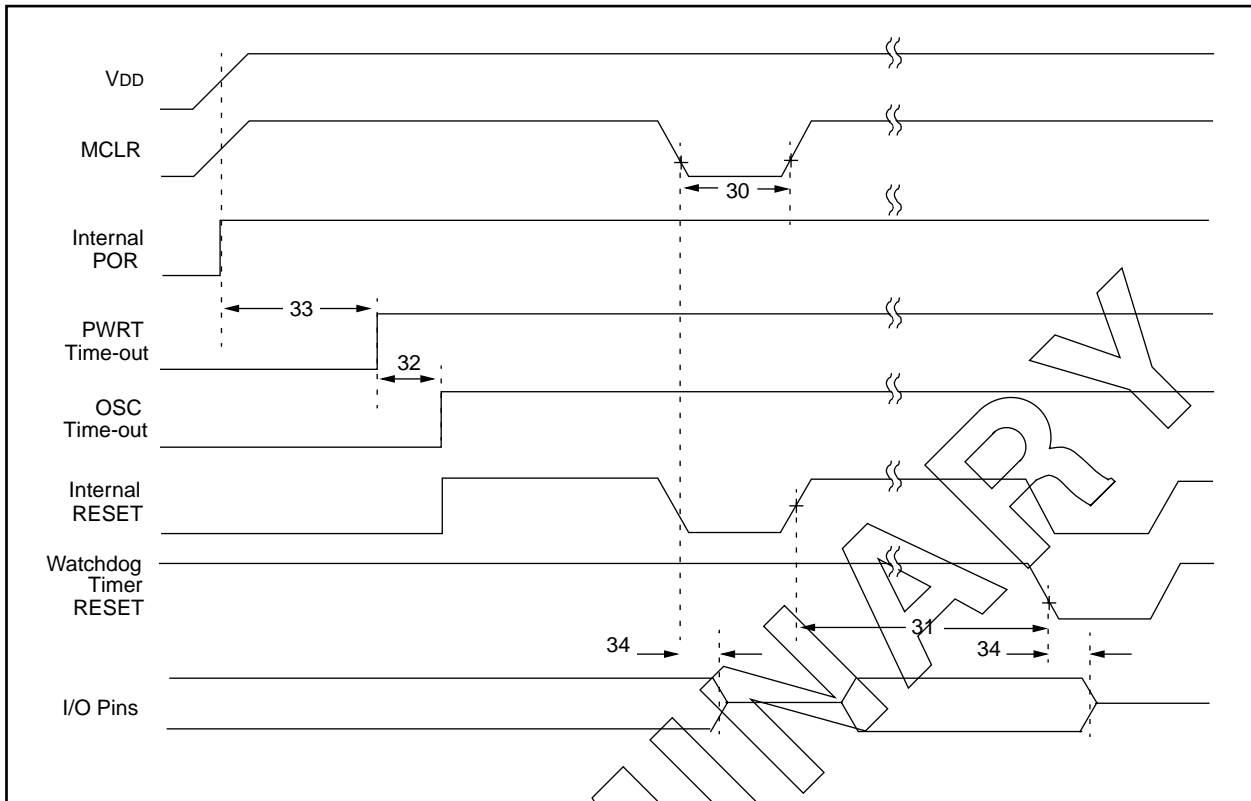


TABLE 9-5 RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	2 *	—	—	μs	VDD = 5.0V, extended
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7 *	18	33 *	ms	VDD = 5.0V, extended
32	Tost	Oscillation Start-up Timer Period	—	1024Tosc	—	ms	Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period	28 *	72	132 *	ms	VDD = 5.0V, extended
34	Tioz	I/O Hi-impedance from MCLR Low or reset	—	—	100 *	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16F84A

FIGURE 9-6: TIMER0 CLOCK TIMINGS

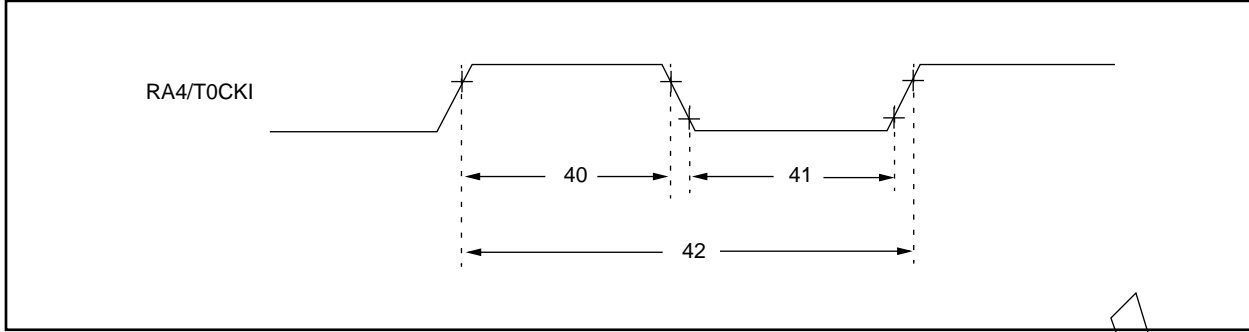


TABLE 9-6 TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	0.5TCY + 20 *	—	—	ns	
		No Prescaler					
		With Prescaler	50 *	—	—	ns	2.0V ≤ VDD ≤ 3.0V
			30 *	—	—	ns	3.0V ≤ VDD ≤ 6.0V
41	Tt0L	T0CKI Low Pulse Width	0.5TCY + 20 *	—	—	ns	
		No Prescaler					
		With Prescaler	50 *	—	—	ns	2.0V ≤ VDD ≤ 3.0V
			20 *	—	—	ns	3.0V ≤ VDD ≤ 6.0V
42	Tt0P	T0CKI Period	TCY + 40 *	—	—	ns	N = prescale value (2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PRELIMINARY

10.0 DC & AC CHARACTERISTICS GRAPHS/TABLES

No data available at this time.

PRELIMINARY

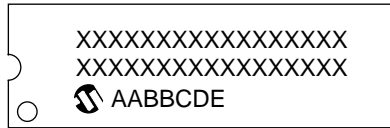
PIC16F84A

NOTES:

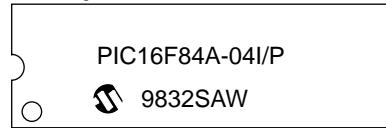
11.0 PACKAGING INFORMATION

11.1 Package Marking Information

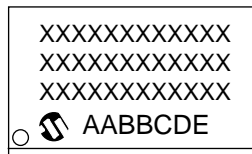
18L PDIP



Example



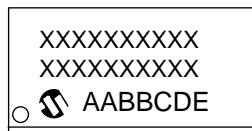
18L SOIC



Example



20L SSOP



Example

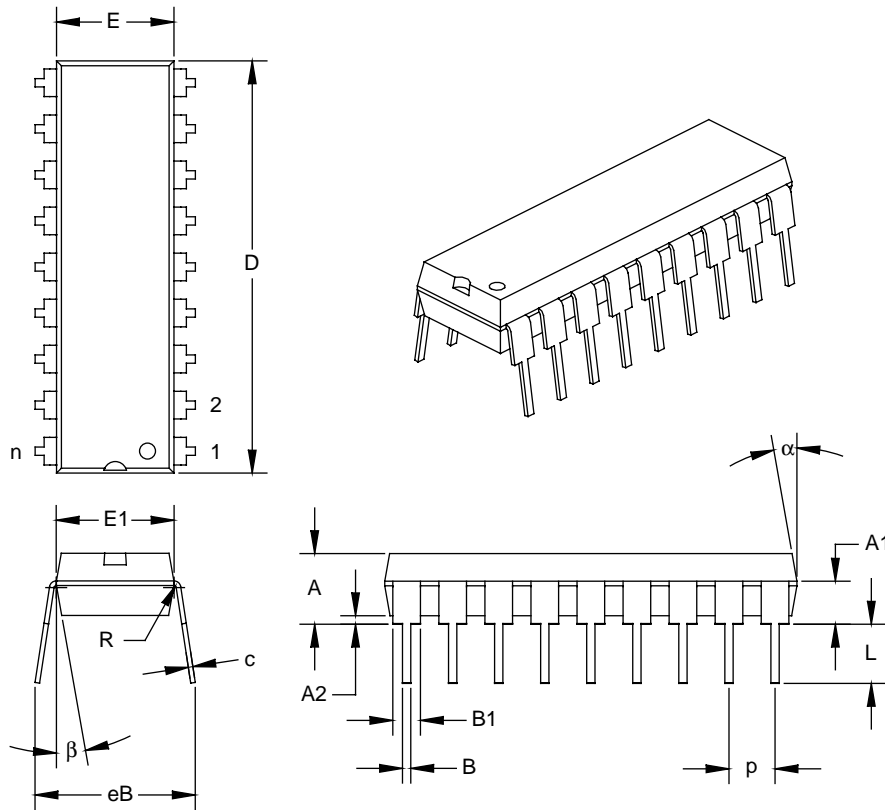


Legend: MM...M	Microchip part number information
XX...X	Customer specific information*
AA	Year code (last 2 digits of calendar year)
BB	Week code (week of January 1 is week '01')
C	Facility code of the plant at which wafer is manufactured
	O = Outside Vendor
	C = 5" Line
	S = 6" Line
	H = 8" Line
D	Mask revision number
E	Assembly code of the plant or country of origin in which part was assembled
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

PIC16F84A

11.2 K04-007 18-Lead Plastic Dual In-line (P) – 300 mil



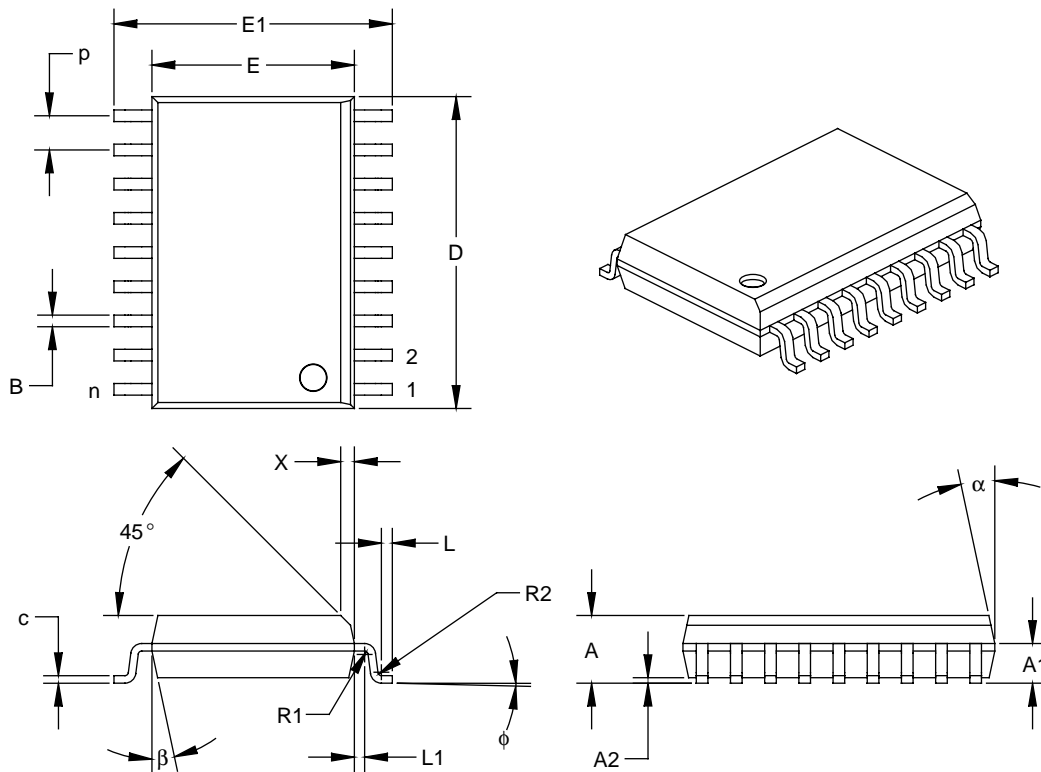
Units		INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Dimension Limits							
PCB Row Spacing			0.300			7.62	
Number of Pins	n		18			18	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.013	0.018	0.023	0.33	0.46	0.58
Upper Lead Width	B1†	0.055	0.060	0.065	1.40	1.52	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.005	0.010	0.015	0.13	0.25	0.38
Top to Seating Plane	A	0.110	0.155	0.155	2.79	3.94	3.94
Top of Lead to Seating Plane	A1	0.075	0.095	0.115	1.91	2.41	2.92
Base to Seating Plane	A2	0.000	0.020	0.020	0.00	0.51	0.51
Tip to Seating Plane	L	0.125	0.130	0.135	3.18	3.30	3.43
Package Length	D‡	0.890	0.895	0.900	22.61	22.73	22.86
Molded Package Width	E‡	0.245	0.255	0.265	6.22	6.48	6.73
Radius to Radius Width	E1	0.230	0.250	0.270	5.84	6.35	6.86
Overall Row Spacing	eB	0.310	0.349	0.387	7.87	8.85	9.83
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

11.3 K04-051 18-Lead Plastic Small Outline (SO) – Wide, 300 mil



Units	Dimension Limits	INCHES*			MILLIMETERS			
		MIN	NOM	MAX	MIN	NOM	MAX	
	Pitch	p	0.050			1.27		
	Number of Pins	n	18			18		
	Overall Pack. Height	A	0.093	0.099	0.104	2.36	2.50	2.64
	Shoulder Height	A1	0.048	0.058	0.068	1.22	1.47	1.73
	Standoff	A2	0.004	0.008	0.011	0.10	0.19	0.28
	Molded Package Length	D [†]	0.450	0.456	0.462	11.43	11.58	11.73
	Molded Package Width	E [‡]	0.292	0.296	0.299	7.42	7.51	7.59
	Outside Dimension	E1	0.394	0.407	0.419	10.01	10.33	10.64
	Chamfer Distance	X	0.010	0.020	0.029	0.25	0.50	0.74
	Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
	Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
	Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
	Foot Angle	φ	0	4	8	0	4	8
	Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
	Lead Thickness	c	0.009	0.011	0.012	0.23	0.27	0.30
	Lower Lead Width	B [†]	0.014	0.017	0.019	0.36	0.42	0.48
	Mold Draft Angle Top	α	0	12	15	0	12	15
	Mold Draft Angle Bottom	β	0	12	15	0	12	15

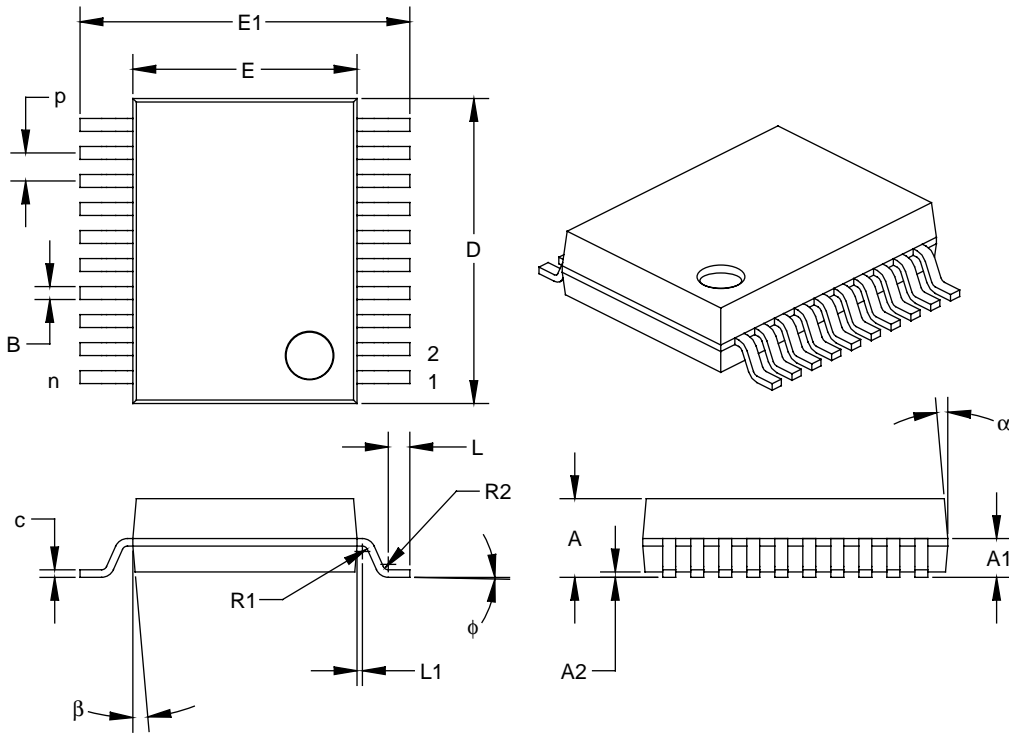
* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

PIC16F84A

11.4 K04-072 20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm



Units	Dimension Limits	INCHES			MILLIMETERS*			
		MIN	NOM	MAX	MIN	NOM	MAX	
	Pitch	p	0.026		0.65			
	Number of Pins	n	20		20			
	Overall Pack. Height	A	0.068	0.073	0.078	1.73	1.86	1.99
	Shoulder Height	A1	0.026	0.036	0.046	0.66	0.91	1.17
	Standoff	A2	0.002	0.005	0.008	0.05	0.13	0.21
	Molded Package Length	D [†]	0.278	0.283	0.289	7.07	7.20	7.33
	Molded Package Width	E [‡]	0.205	0.208	0.212	5.20	5.29	5.38
	Outside Dimension	E1	0.301	0.306	0.311	7.65	7.78	7.90
	Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
	Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
	Foot Length	L	0.015	0.020	0.025	0.38	0.51	0.64
	Foot Angle	ϕ	0	4	8	0	4	8
	Radius Centerline	L1	0.000	0.005	0.010	0.00	0.13	0.25
	Lead Thickness	c	0.005	0.007	0.009	0.13	0.18	0.22
	Lower Lead Width	B [†]	0.010	0.012	0.015	0.25	0.32	0.38
	Mold Draft Angle Top	α	0	5	10	0	5	10
	Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

[†] Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

[‡] Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

APPENDIX A: REVISION HISTORY

Version	Date	Revision Description
A	9/14/98	This is a new data sheet. However, the devices described in this data sheet are the upgrades to the devices found in the <i>PIC16F8X Data Sheet</i> , DS30430C.

APPENDIX B: CONVERSION CONSIDERATIONS

Considerations for converting from one PIC16X8X device to another are listed in Table B-1.

TABLE B-1: CONVERSION CONSIDERATIONS - PIC16C84, PIC16F83/F84, PIC16CR83/CR84, PIC16F84A

Difference	PIC16C84	PIC16F83/F84	PIC16CR83/CR84	PIC16F84A
Program Memory size	1k x 14	512 x 14 / 1k x 14	512 x 14 / 1k x 14	1k x 14
Data Memory size	36 x 8	36 x 8 / 68 x 8	36 x 8 / 68 x 8	68 x 8
Voltage Range	2.0V - 6.0V (-40°C to +85°C)	2.0V - 6.0V (-40°C to +85°C)	2.0V - 6.0V (-40°C to +85°C)	2.0V - 5.5V (-40°C to +125°C)
Maximum Operating Frequency	10MHz	10MHz	10MHz	20MHz
Supply Current (IDD). See parameter # D014 in the electrical spec's for more detail.	IDD (typ) = 60µA IDD (max) = 400µA (LP osc, FOSC = 32kHz, VDD = 2.0V, WDT disabled)	IDD (typ) = 15µA IDD (max) = 45µA (LP osc, FOSC = 32kHz, VDD = 2.0V, WDT disabled)	IDD (typ) = 15µA IDD (max) = 45µA (LP osc, FOSC = 32kHz, VDD = 2.0V, WDT disabled)	IDD (typ) = 15µA IDD (max) = 45µA (LP osc, FOSC = 32kHz, VDD = 2.0V, WDT disabled)
Power-down Current (IPD). See parameters # D020, D021, and D021A in the electrical spec's for more detail.	IPD (typ) = 26µA IPD (max) = 100µA (VDD = 2.0V, WDT disabled, industrial)	IPD (typ) = 0.4µA IPD (max) = 9µA (VDD = 2.0V, WDT disabled, industrial)	IPD (typ) = 0.4µA IPD (max) = 6µA (VDD = 2.0V, WDT disabled, industrial)	IPD (typ) = 0.4µA IPD (max) = 9µA (VDD = 2.0V, WDT disabled, industrial)
Input Low Voltage (VIL). See parameters # D032 and D034 in the electrical spec's for more detail.	VIL (max) = 0.2VDD (Osc1, RC mode)	VIL (max) = 0.1VDD (Osc1, RC mode)	VIL (max) = 0.1VDD (Osc1, RC mode)	VIL (max) = 0.1VDD (Osc1, RC mode)
Input High Voltage (VIH). See parameter # D040 in the electrical spec's for more detail.	VIH (min) = 0.36VDD (I/O Ports with TTL, 4.5V ≤ VDD ≤ 5.5V)	VIH (min) = 2.4V (I/O Ports with TTL, 4.5V ≤ VDD ≤ 5.5V)	VIH (min) = 2.4V (I/O Ports with TTL, 4.5V ≤ VDD ≤ 5.5V)	VIH (min) = 2.4V (I/O Ports with TTL, 4.5V ≤ VDD ≤ 5.5V)
Data EEPROM Memory Erase/Write cycle time (TDEW). See parameter # D122 in the electrical spec's for more detail.	TDEW (typ) = 10ms TDEW (max) = 20ms	TDEW (typ) = 10ms TDEW (max) = 20ms	TDEW (typ) = 10ms TDEW (max) = 20ms	TDEW (typ) = 4ms TDEW (max) = 10ms

PIC16F84A

TABLE B-1: CONVERSION CONSIDERATIONS - PIC16C84, PIC16F83/F84, PIC16CR83/CR84, PIC16F84A

Difference	PIC16C84	PIC16F83/F84	PIC16CR83/CR84	PIC16F84A
Port Output Rise/Fall time (TioR, TioF). See parameters #20, 20A, 21, and 21A in the electrical spec's for more detail.	TioR, TioF (max) = 25ns (C84) TioR, TioF (max) = 60ns (LC84)	TioR, TioF (max) = 35ns (C84) TioR, TioF (max) = 70ns (LC84)	TioR, TioF (max) = 35ns (C84) TioR, TioF (max) = 70ns (LC84)	TioR, TioF (max) = 35ns (C84) TioR, TioF (max) = 70ns (LC84)
MCLR on-chip filter. See parameter #30 in the electrical spec's for more detail.	No	Yes	Yes	Yes
PORTA and crystal oscillator values less than 500kHz	For crystal oscillator configurations operating below 500kHz, the device may generate a spurious internal Q-clock when PORTA<0> switches state.	N/A	N/A	N/A
RB0/INT pin	TTL	TTL/ST* (* Schmitt Trigger)	TTL/ST* (* Schmitt Trigger)	TTL/ST* (* Schmitt Trigger)
EEADR<7:6> and IDD	It is recommended that the EEADR<7:6> bits be cleared. When either of these bits is set, the maximum IDD for the device is higher than when both are cleared.	N/A	N/A	N/A
The polarity of the PWRTE bit	PWRTE	PWRTE	PWRTE	PWRTE
Recommended value of REXT for RC oscillator circuits	REXT = 3kΩ - 100kΩ	REXT = 5kΩ - 100kΩ	REXT = 5kΩ - 100kΩ	REXT = 3kΩ - 100kΩ
GIE bit unintentional enable	If an interrupt occurs while the Global Interrupt Enable (GIE) bit is being cleared, the GIE bit may unintentionally be re-enabled by the user's Interrupt Service Routine (the RETFIE instruction).	N/A	N/A	N/A
Packages	PDIP, SOIC	PDIP, SOIC	PDIP, SOIC	PDIP, SOIC, SSOP

NOTES:

APPENDIX C: MIGRATION FROM BASELINE TO MIDRANGE DEVICES

This section discusses how to migrate from a baseline device (i.e., PIC16C5X) to a midrange device (i.e., PIC16CXXX).

The following is the list of feature improvements over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14 bits. This allows larger page sizes both in program memory (2K now as opposed to 512 before) and the register file (128 bytes now versus 32 bytes before).
2. A PC latch register (PCLATH) is added to handle program memory paging. PA2, PA1 and PA0 bits are removed from the status register and placed in the option register.
3. Data memory paging is redefined slightly. The STATUS register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW. Two instructions, TRIS and OPTION, are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers, the Oscillator Start-up Timer (OST) and Power-up Timer (PWRT), are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt on change features.
13. T0CKI pin is also a port pin (RA4/T0CKI).
14. FSR is a full 8-bit register.
15. "In system programming" is made possible. The user can program PIC16CXX devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).

To convert code written for PIC16C5X to PIC16F84A, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables for reallocation.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.

INDEX

A

Absolute Maximum Ratings	41
AC (Timing) Characteristics	47
Architecture, Block Diagram	3
Assembler	
MPASM Assembler	37

B

Banking, Data Memory	6, 8
----------------------------	------

C

CLKIN Pin	4
CLKOUT Pin	4
Code Protection	21, 32
Configuration Bits	21
Conversion Considerations	59

D

Data EEPROM Memory	19
EEADR Register	7, 24
EECON1 Register	7, 19, 24
EECON2 Register	7, 19, 24
EEDATA Register	7, 24
Write Complete Enable (EEIE Bit)	10, 29
Write Complete Flag (EEIF Bit)	19, 29
Data EEPROM Write Complete	29
Data Memory	6
Bank Select (RP0 Bit)	6, 8
Banking	6
DC & AC Characteristics Graphs/Tables	53
DC Characteristics	43, 44, 45, 46
Development Support	35
Development Tools	35

E

EECON1 Register	19
EEIF Bit	19, 29
RD Bit	19
WR Bit	19
WREN Bit	19
WRERR Bit	19
Electrical Characteristics	41
Endurance	1
Errata	2
External Power-on Reset Circuit	25

F

Firmware Instructions	33
ftp site	65
Fuzzy Logic Dev. System (<i>fuzzyTECH</i> [®] -MP)	37

I

I/O Ports	13
ICEPIC Low-Cost PIC16CXXX In-Circuit Emulator	35
ID Locations	21, 32
In-Circuit Serial Programming (ICSP)	21, 32
Indirect Addressing	11
FSR Register	6, 7, 11, 24
INDF Register	7, 24
Instruction Format	33
Instruction Set	33
Summary Table	34
INT Interrupt (RB0/INT)	29

INTCON Register	7, 10, 18, 24, 28
EEIE Bit	10, 29
GIE Bit	10, 28, 29
INTE Bit	10, 29
INTF Bit	10, 29
RBIE Bit	10, 29
RBIF Bit	10, 15, 29
TOIE Bit	10, 29
TOIF Bit	10, 18, 29
Interrupt Sources	21, 28
Block Diagram	28
Data EEPROM Write Complete	28, 31
Interrupt on Change (RB7:RB4)	4, 15, 28, 31
RB0/INT Pin, External	4, 16, 28, 31
TMR0 Overflow	18, 28
Interrupts, Context Saving During	29
Interrupts, Enable Bits	
Data EEPROM Write Complete Enable (EEIE Bit)	10, 29
Global Interrupt Enable (GIE Bit)	10
Interrupt on Change (RB7:RB4) Enable (RBIE Bit)	10
RB0/INT Enable (INTE Bit)	10
TMR0 Overflow Enable (TOIE Bit)	10
Interrupts, Flag Bits	28
Data EEPROM Write Complete Flag (EEIF Bit)	19, 29
Interrupt on Change (RB7:RB4) Flag (RBIF Bit)	10
RB0/INT Flag (INTF Bit)	10
TMR0 Overflow Flag (TOIF Bit)	10

K

KeeLoq [®] Evaluation and Programming Tools	38
--	----

M

Master Clear ($\overline{\text{MCLR}}$)	
MCLR Pin	4
$\overline{\text{MCLR}}$ Reset, Normal Operation	23
$\overline{\text{MCLR}}$ Reset, SLEEP	23, 31
Memory Organization	5
Data EEPROM Memory	19
Data Memory	6
Program Memory	5
Migration from Baseline to Midrange Devices	62
MPLAB Integrated Development Environment	
Software	37

O

On-Line Support	65
OPCODE Field Descriptions	33
OPTION_REG Register	7, 9, 16, 18, 24
INTEDG Bit	9, 29
PS2:PS0 Bits	9, 17
PSA Bit	9, 17
RBPV Bit	9
T0CS Bit	9
T0SE Bit	9
OSC1 Pin	4
OSC2 Pin	4
Oscillator Configuration	21, 22
HS	22, 28
LP	22, 28
RC	22, 23, 28
Selection (FOSC1:FOSC0 Bits)	21
XT	22, 28

PIC16F84A

P

Packaging	55
PICDEM-1 Low-Cost PICmicro Demo Board	36
PICDEM-2 Low-Cost PIC16CXX Demo Board	36
PICDEM-3 Low-Cost PIC16CXX Demo Board	36
PICSTART® Plus Entry Level Development System	35
Pinout Descriptions	4
Pointer, FSR	11
PORTA	4, 13
Initializing	13
PORTA Register	7, 13, 14, 24
RA3:RA0 Block Diagram	13
RA4 Block Diagram	14
RA4/T0CKI Pin	4, 13, 17
TRISA Register	7, 13, 14, 18, 24
PORTB	4, 15
Initializing	15
PORTB Register	7, 15, 16, 24
Pull-up Enable (RBP \bar{U} Bit)	9
RB0/INT Edge Select (INTEDG Bit)	9
RB0/INT Pin, External	4, 16, 29
RB3:RB0 Block Diagram	15
RB7:RB4 Block Diagram	15
RB7:RB4 Interrupt on Change	4, 15, 29
RB7:RB4 Interrupt on Change Enable (RBIE Bit)	10
RB7:RB4 Interrupt on Change Flag (RBIF Bit)	10, 15
TRISB Register	7, 15, 16, 24
Power-on Reset (POR)	21, 23, 25
Oscillator Start-up Timer (OST)	21, 25
P \bar{D} Bit	8, 23, 28, 31, 32, 34
Power-up Timer (PWRT)	21, 25
PWRT Enable (PWRT \bar{E} Bit)	21
Time-out Sequence	28
Time-out Sequence on Power-up	26, 27
T \bar{O} Bit	8, 23, 28, 30, 31, 32, 34
Prescaler	17
Assignment (PSA Bit)	9, 17
Block Diagram	18
Rate Select (PS2:PS0 Bits)	9, 17
Switching Prescaler Assignment	18
PRO MATE® II Universal Programmer	35
Product Identification System	67
Program Counter	11
PCL Register	7, 11, 24
PCLATH Register	7, 11, 24
Reset Conditions	24
Program Memory	5
General Purpose Registers	6
Interrupt Vector	5, 29
Reset Vector	5
Special Function Registers	6, 7
Programming, Device Instructions	33

R

RAM. See Data Memory	
Reader Response	66
Register File	6
Reset	21, 23
Block Diagram	23
Reset Conditions for All Registers	24
Reset Conditions for Program Counter	24
Reset Conditions for STATUS Register	24
WDT Reset. See Watchdog Timer (WDT)	
Revision History	59

S

Saving W Register and STATUS in RAM	29
SEEVAL® Evaluation and Programming System	37
SLEEP	21, 23, 29, 31
Software Simulator (MPLAB-SIM)	37
Special Features of the CPU	21
Special Function Registers	6, 7
Speed, Operating	1, 22, 49
Stack	11
STATUS Register	7, 8, 24, 29
C Bit	8, 34
DC Bit	8, 34
P \bar{D} Bit	8, 23, 28, 31, 32, 34
Reset Conditions	24
RP0 Bit	6, 8
T \bar{O} Bit	8, 23, 28, 30, 31, 32, 34
Z Bit	8, 34

T

Time-out (T \bar{O}) Bit. See Power-on Reset (POR)	
Timer0	17
Block Diagram	17
Clock Source Edge Select (T0SE Bit)	9
Clock Source Select (T0CS Bit)	9
Overflow Enable (T0IE Bit)	10, 29
Overflow Flag (T0IF Bit)	10, 18, 29
Overflow Interrupt	18, 29
RA4/T0CKI Pin, External Clock	17
TMR0 Register	7, 18, 24
Timing Diagrams	
Diagrams and Specifications	49
Time-out Sequence on Power-up	26, 27

W

W Register	24, 29
Wake-up from SLEEP	21, 25, 28, 29, 31
Interrupts	31, 32
MCLR Reset	31
WDT Reset	31
Watchdog Timer (WDT)	21, 30
Block Diagram	30
Enable (WDTE Bit)	21
Programming Considerations	30
RC Oscillator	30
Time-out Period	30
WDT Reset, Normal Operation	23
WDT Reset, SLEEP	23, 31
WWW, On-Line Support	2, 65

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PIC16F84A

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